Optimal Implementation of Sea of Leads (SoL) Compliant Interconnect Technology

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Abstract

Compliant interconnects can enable wafer level packages to provide high I/O density, high reliability and better performance with low cost and small size. A fabrication process for SoL compliant interconnects has been optimized to achieve high yield and compatibility with standard back-end-of-line (BEOL) as well as flip-chip bonding processes. The optimized fabrication process further enables a reliable joining between the IC with SoL compliant interconnects to the next level of packaging without the use of an expensive underfilling process.

I. Introduction

According to the International Technology Roadmap of Semiconductor (ITRS) 2002 [1], chip-to-substrate or off-chip interconnect pitch is to be scaled down to 40~90μm in 2016 to provide very high area array interconnect density. As a result, the dimension of the C4 solder joints in flip-chip packages must be reduced to less than 50μm. Shear strain on a C4 joint induced by CTE mismatch between Si and organic PWB substrate will then increase significantly when the stand-off height becomes smaller. Although underfill is widely used to reduce the magnitude of the shear strain on the C4 joints today, underfilling will be more and more difficult for such a small gap between chip and substrate. Compliant interconnects can be fabricated in wafer level and compensate for the CTE mismatch between Si chip and organic PWB substrate, thus eliminate the need for underfill. Another motivation for compliant interconnects comes from application of low-k dielectric. The mechanical strength of the porous low-k dielectric materials is weak enough to cause delamination of bonding pads due to a high strain on the C4 joints [2].

Among several compliant interconnect technologies [2-5], SoL has great potential to provide a high density I/O interconnect at low cost since SoL technology simply extends BEOL with a few steps in wafer level. It has been found that the added cost of SoL is small [6,7]. To implement SoL to be fully compatible with BEOL process as well as the standard flip-chip assembly process, several issues must be addressed. First of all, in the previous study [5], an undercut process involving wet etching has been used to partially release the interconnect leads from adhering to chip passivation (Si_3N_4 or polymer) so that partially released leads are able to give required compliance. However, such process requires a careful design of lead dimensions and a timed etching process to avoid detaching of leads from chip pads. In practice, precise control of the wet etching undercut rate across a Si wafer is difficult, especially when a Si wafer moves into 300mm regime. In addition, a reliable under-bump-metallization (UBM) is required for solder joints to provide strong bonding with the compliant leads. A well-known reliability issue in conventional C4 technology is the excessive growth of Cu-Sn intermetallics during reflow, storage and operation at elevated temperature [8,9]. Growth of Cu-Sn intermetallics results in a brittle joining interface between C4 solder bump and chip metallization. In contrast, Ni-Sn intermetallics provide strong bonding and grow at a relatively slower rate, which makes Ni-based UBM very attractive [9]. Therefore, it is desirable to apply a Ni-based UBM for SoL. Finally, a suitable solder barrier/dam must be applied to protect the compliant leads because solder wicking may occur when solder is in contact with the lead during soldering process. To address these issues, the fabrication processes need to be optimized and a complete bumping solution for SoL needs to be developed based on the previous studies [5-7].

In this work, the fabrication process of SoL has been optimized to achieve high yield, high reliability and high I/O density compliant interconnect technology. An etch-stop undercut process has been developed to produce flexible leads without affecting the end of a lead that is anchored on a chip pad. The optimized process also allows electroplated Ni to be applied on the compliant leads as a reliable UBM for C4 solder bumps. A layer of Ti/SiO_2 can serve as a solder barrier surrounding a C4 solder bump. To further protect the sidewall of a metal lead, an enhanced solder dam has been fabricated with dielectric polymer.

II. Optimization of SoL Fabrication Process

As shown in Fig.1a, fabrication of SoL begins with a completed wafer with final via through final passivation (Si_3N_4 or polymer). The proposed process requires a sacrificial layer to be deposited and patterned with the via mask (Fig.1b) before the seed layer is sputtered. A seed layer of Ti/Cu (30nm/200nm) is then deposited for electroplating (Fig.1c). Metal leads are formed in a photoresist mold defined by photolithographic process (Fig.1d). The seed layer provides a strong adhesion for the electroplated leads at a via. After photoresist is stripped, the seed layer is removed by wet etching in vertical direction (Fig.1e). The next step is to release the electroplated leads by undercut etching of the sacrificial layer (Fig.1f). Al film is a good option as a sacrificial layer because it can be selectively etched by diluted NaOH solution, which is benign to the electroplated metal leads as well as the adhesion layer.

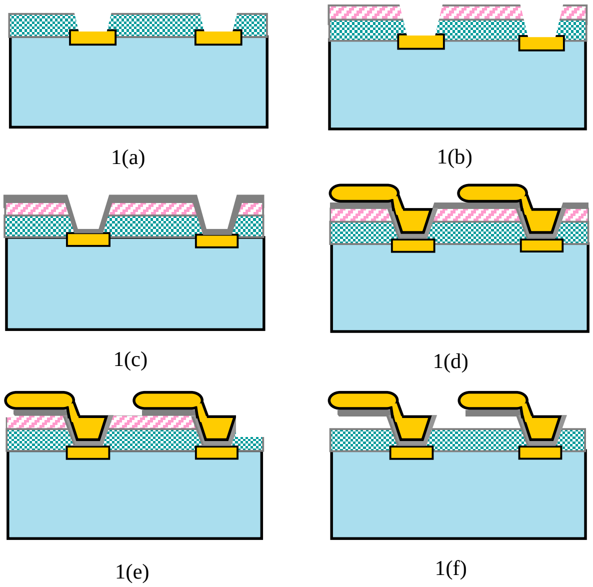
1(a) 1(b)
1(c) 1(d)
1(e) 1(f)

Figure 1. Illustration of electroplating process of SoL and lead release process by sacrificial layer undercut etching

To confirm such a process is successful, a destructive peeling test has been performed with adhesive tape. Fig. 2 clearly indicates that the metal leads have been successfully released from adhering on the final passivation after the sacrificial layer is etched. Meanwhile, the via end of a lead is still well anchored although it is partially released. It is because there is no sacrificial layer beneath the seed layer (adhesion layer) at via end of a plated lead, anchoring of a lead will not be affected by the undercut etching process. This is a key improvement based on the previous undercut process described in [5].

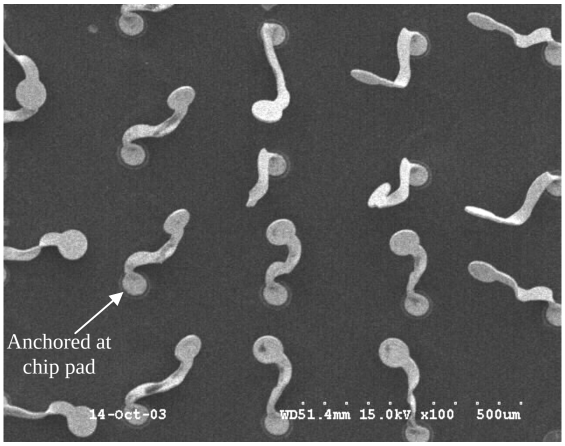

Figure 2. SEM photograph of SoL after release process: destructive peeling test confirms that leads are flexible but well-anchored

III. Bumping Process of SoL Compliant Interconnect

In general, critical elements of a solder bumping process include a reliable UBM, a controlled volume of solder as well as a solder dam/barrier. Similar to the conventional C4 bumping process, SnPb solder bumps can be deposited on the compliant leads by electroplating. As illustrated in Fig.3, the upper end of each lead serves as a C4 land and a Ti/Cu/Ni/SnPb structure is used for bumping. A ring of Ti/SiO_2 is first deposited and patterned to act as a solder barrier (Fig.3a). A Ti/Cu (100nm/200nm) layer is then sputtered to act as an adhesion layer and seed layer. A negative resist with thickness of 35μm is used to produce the mold for electroplating. A 3μm Ni layer is first electroplated as UBM (Fig.3b). After an acid cleaning step, solder bumps with mushroom shape are electroplated directly over the Ni UBM (Fig.3c). In this manner, a clean interface between the UBM and the solder alloy is ensured, which is critical for an excellent wettability. After reflow with flux, a solder bump with spherical shape is formed and strong bonding of the solder bump with the compliant lead is achieved (Fig.3d).

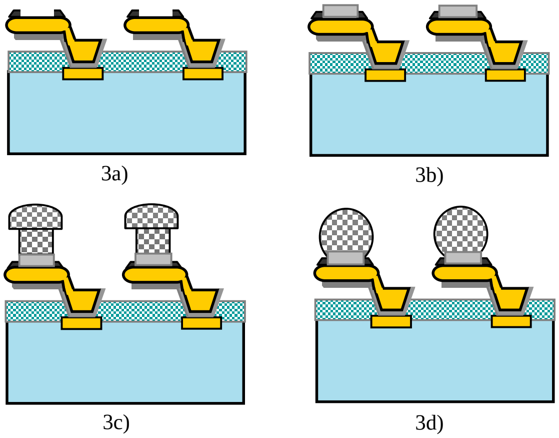
3a) 3b)
3c) 3d)

Figure 3. Illustration of the bumping process by electroplating for the compliant leads.

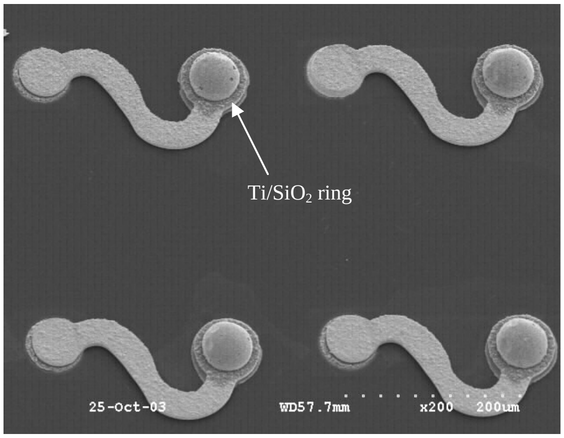

Figure 4. SEM photograph of bumped leads with a Ti/SiO_2 ring as solder barrier

An image of the completed compliant Au leads with solder barrier rings and UBM is shown in Fig. 4. Solder barrier ring is critical to confine the wetting area of C4 solder bump and protect the Au lead from being wicked by solder during reflow.

IV. Sidewall Protection for Flip-Chip Bonding

In the case of flip-chip bonding for a SoL chip, the solder dam is particularly required to prevent leads from being wicked because the bulk lead is Au. A compressive bonding can push the molten solder to be squeezed in lateral directions and may cause wetting of sidewalls of a lead. Therefore, a new approach to sidewall protection is proposed. Using a photodefineable dielectric polymer (Avatrel 2000, Promerus, LLC.), a solder dam is fabricated by a photolithographic step as shown in Fig. 5. After curing of the polymer at 200°C, a descum process is performed to ensure a clean surface for C4 solder bump sites and the wafer is ready for bumping processed described above.

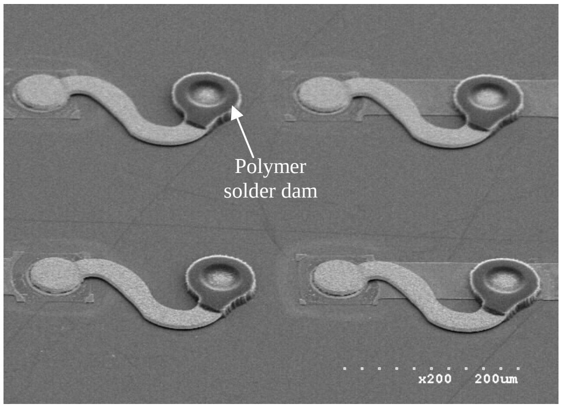

Figure 5. Photodefined polymer solder dam on the compliant leads to cover the sidewall and prevent solder wicking.

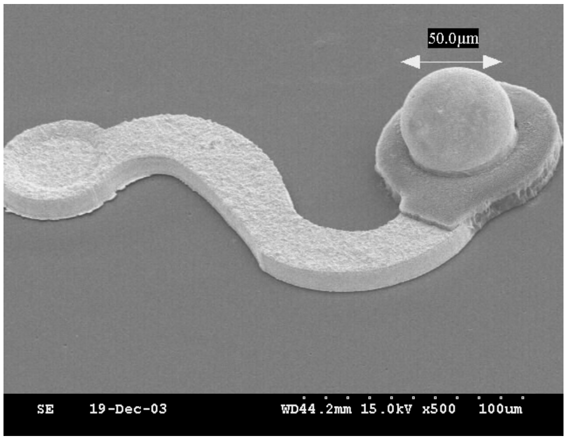

Figure 6. SEM photograph of a reflowed solder bump on a electroplated metal lead which is protected by a photodefined polymer dam. (The diameter of the solder ball is 50μm)

Fig. 6 shows the successfully reflowed SnPb solder ball surrounded by the dielectric polymer dam. Since the polymer dam effectively covers sidewall of the C4 land, solder wicking is unlikely to occur even during compressive bonding process.

V. Conclusion

A SoL fabrication process has been optimized for integration into a standard BEOL process that involves an etch-stop undercut of a sacrificial layer to produce highly reliable compliant leads. Furthermore, a Ni-based UBM has been applied to provide strong bonding with the compliant leads to enhance the reliability of SoL when it is bonded to the next level of packaging. An enhanced solder dam has been fabricated with Ti/SiO_2 and photodefinable dielectric polymer to completely prevent solder wicking during flip chip bonding process. The resulting SoL structure provides a low-cost, high-yield and high I/O density compliant interconnect technology that can be easily integrated with standard BEOL process.

Acknowledgements

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