

A Comparative Study of Threshold Variations in Symmetric and Asymmetric Undoped Double-Gate MOSFETs

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I. Introduction*

For the purpose of giga-scale integration with double-gate (DG) MOSFET technology, it is imperative to consider parameter variations. In this paper, analytical long-channel and short-channel threshold voltage (V_{TH}) models for undoped asymmetric DG (ADG) MOSFETs are developed to reveal V_{TH} dependencies on device dimensions. Using the quantitative scaling theory [1], V_{TH} variations of ADG MOSFETs are then comprehensively investigated and compared to those of symmetric DG (SDG) MOSFETs recently studied in [1]. ADG MOSFETs with p+/n+ poly or equivalent gates are used for case studies. It is found that threshold variations in nearly ideal, long-channel ADG devices are 10x as large as those in SDG devices.

II. Long-Channel V_{TH} Model

In a long-channel ADG MOSFET, the channel potential profile under threshold conditions has a nearly constant slope. Based on this observation, a compact, analytical V_{TH} model is developed,

$$V_{TH,Long} = \frac{kT}{q} \ln \frac{Q_{TH}}{n_i t_{Si}} + \frac{kT}{q} \ln \left(\frac{r}{r+2} \frac{q \Phi_{ABV}}{kT} \right) + \frac{(r+1) \Phi_{MS,i,F} + \Phi_{MS,i,B}}{r+2}, \quad (1)$$

where Q_{TH} is a constant sheet density of mobile carriers at which V_{TH} is measured. Such a V_{TH} definition is a close equivalent of the widely used constant-drain-current methodology. Other parameters of (1) are given in Table I. Model (1) agrees well with Medici numerical simulations (Figure 1). ADG has a much stronger V_{TH} dependence on silicon film thickness (t_{Si}) than SDG (see inset of Figure 1 [1]). That is because t_{Si} impacts V_{TH} in ADG through the slope of the potential profile, while it affects V_{TH} in SDG only through volume inversion. The reduction of V_{TH} with gate oxide thickness (t_{ox}) in ADG (Figure 1) is caused by a reduced voltage drop across the gate oxide when t_{ox} decreases, so that a lower gate voltage is needed to turn on the device. This mechanism is similar to that in conventional bulk MOSFETs.

III. Short-Channel V_{TH} Model

The short-channel V_{TH} model is derived by solving the two-dimensional Poisson equation in the channel,

$$V_{TH} = \Phi_{MS,i,F} + \phi_{max} + (kT/q) n_i t_{Si} \exp(q \phi_{max} / kT) / Q_{TH} r. \quad (2)$$

Parameters of (2) are given in Table I. Encouraging agreement between the model and Medici simulations is obtained (Figure 2). Following the *quantitative* scaling theory [1], the rolloff characteristics in Figure 2 can be unified dividing the channel length (L) by the scale length λ_1 [2], resulting in a unique rolloff dependence on the ratio of L/λ_1 (Figure 3). Thus, the ratio L/λ_1 serves as a quantitative measure of short-channel effects.

IV. Threshold Voltage Variations

Based on the quantitative scaling theory, a unique approach was recently developed and successfully applied to study threshold variations (δV_{TH}) of SDG [1]. It is to study δV_{TH} caused by process tolerances of device dimensions (expressed in percentage, for example, 10%) as unique functions of the ratio L/λ_1 . This same approach will be exploited here to comprehensively investigate δV_{TH} of ADG.

V_{TH} sensitivity to t_{Si} (Figure 4). δV_{TH} per 10% t_{Si} tolerance is about 13 mV in long-channel ADG, 5x that in SDG, as explained in Section II. δV_{TH} becomes comparable in ADG and SDG at deep short-channel designs when L/λ_1 drops below 3.8.

V_{TH} sensitivity to L (Figure 5). This sensitivity in ADG is slightly smaller than in SDG at an elevated drain bias ($V_{DS}=1V$). It may be explained by a smaller distance between the effective conduction path and the gates in ADG than in SDG [2].

V_{TH} sensitivity to t_{ox} (Figure 6). This sensitivity in long-channel ADG is positive, as explained in Section II. 10% tolerance of t_{ox} causes about 10 mV δV_{TH} in ADG versus ~ 0 in SDG. The sensitivity in ADG is reduced to zero at $L/\lambda_1 \approx 5.4$ and further to negative values with decreasing L (or L/λ_1) as a result of increasing short-channel effects. ADG and SDG have comparable sensitivity at deep short-channel designs when L/λ_1 drops below 3.3.

Overall worst-case V_{TH} variation (Figure 7). It results from the most unfavorable combination of process tolerances of L , t_{Si} and t_{ox} . At short-channel designs with L/λ_1 less than ~ 5.3 , ADG and SDG have nearly identical overall worst-case δV_{TH} . However, at long-channel designs 10% tolerances of t_{Si} and t_{ox} cause ~ 25 mV overall worst-case δV_{TH} in ADG, about 10x that in SDG.

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Decomposition of the overall worst-case δV_{TH} (Figure 8 & Figure 9) reinforces a much greater need of tight control of t_{Si} and t_{ox} in ADG than in SDG.

V. Summary/Conclusions

Threshold variations in ADG caused by process tolerances of L , t_{Si} , and t_{ox} have been comprehensively investigated and compared to those of SDG. In practical designs of p+/n+ ADG, t_{Si} causes 35% to 100% more δV_{TH} than L does for the same process tolerance. For 10% tolerances, the overall worst-case δV_{TH} is nearly identical between SDG and p+/n+ ADG when $L/\lambda_1 \leq 5.3$.

In practical designs, ADG is 1.5x to 2x as susceptible to t_{Si} tolerance as SDG. Tight control of t_{Si} and t_{ox} remains critical for ADG even at long-channel designs.

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References

- [1] Q. Chen, E. M. Harrell, and J. D. Meindl, "A physical short-channel threshold voltage model for undoped symmetric double-gate MOSFETs," sub. *IEEE T-ED*, 2002.
- [2] Q. Chen, B. Agrawal, and J. D. Meindl, "A comprehensive analytical subthreshold swing (S) model for double-gate MOSFETs," *IEEE T-ED*, vol. 49, no. 6, pp. 1086-1090, June 2002.

Table I. Summary of parameters.

<p>n_i is intrinsic density of electrons; $\Phi_{MS,i,F}$ and $\Phi_{MS,i,B}$ are work-functions of front and back gates, referenced to intrinsic silicon; $\Phi_{MM} = \Phi_{MS,i,B} - \Phi_{MS,i,F}$; $r = \epsilon_{ox} t_{Si} / t_{ox} \epsilon_{Si}$; ϵ_{ox} and ϵ_{Si} are permittivity of oxide and silicon, respectively; q is electron charge; k is Boltzmann constant; T is temperature; $V_{bi,i}$ is source junction built-in voltage with intrinsic silicon, and λ_1 is scale length [2].</p> <p>$\phi_{MAX} = (b - \sqrt{b^2 - 4ac}) / 2a$; $a = r + 2$; $b = (r + 2)(V_m - \Phi_{MS,i,F} + \phi_m) + r\Phi_{MM} + \Delta V$; $\Delta V = 0.12V$; $c = (V_{TH} - \Phi_{MS,i,F}) [r(\Phi_{MM} + \phi_m) + 2(\phi_m + \Delta V)] - \Delta V(\Phi_{MM} + \phi_m)$;</p> <p>$\phi_m = V_{TH} - \Phi_{MS,i,F} - \frac{r+1}{r+2}\Phi_{MM} + 2\Gamma_1 \cos \frac{t_{Si}}{2\lambda_1} \sqrt{V_1(V_1 + V_{bi})} e^{-\frac{L}{2\lambda_1}}$; $V_1 = V_{bi} - V_{TH} + \Phi_{MS,i,F} + \Phi_{MM}/2$; $\Gamma_1 = \frac{2\lambda_1}{t_{Si}} \sqrt{1 + \frac{t_{Si}^2}{r^2 \lambda_1^2} / (\frac{1}{r} + \frac{1}{2} + \frac{1}{2} \frac{t_{Si}^2}{r^2 \lambda_1^2})}$; $\tan \frac{t_{Si}}{2\lambda_1} = \frac{r\lambda_1}{t_{Si}}$.</p>

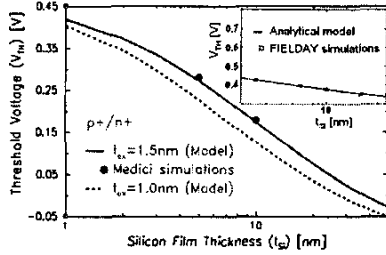


Figure 1. Dependence of long-channel V_{TH} on t_{Si} in ADG. The inset is a similar plot for mid-gap SDG (after [1]).

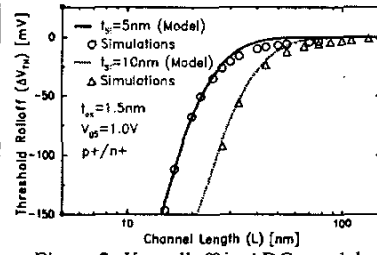


Figure 2. V_{TH} rolloff in ADG: model versus Medici simulations.

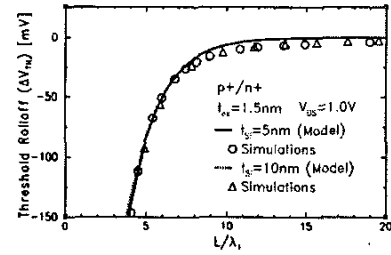


Figure 3. Unified V_{TH} rolloff in ADG, obtained from Figure 2: a unique function of L/λ_1 .

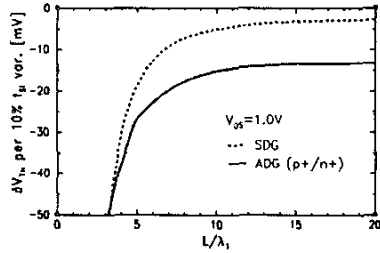


Figure 4. V_{TH} variations per 10% process tolerance of t_{Si} .

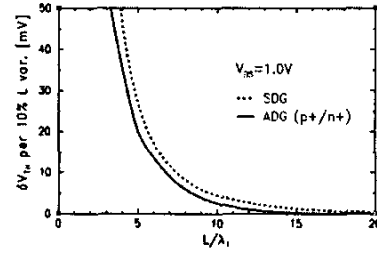


Figure 5. V_{TH} variations per 10% process tolerance of L .

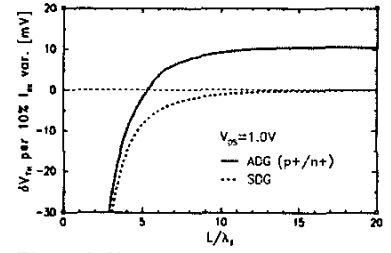


Figure 6. V_{TH} variations per 10% process tolerance of t_{ox} .

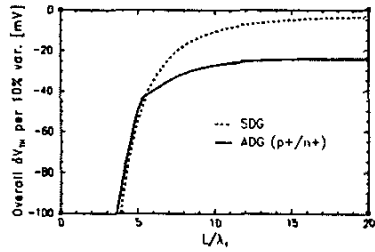


Figure 7. Overall worst-case V_{TH} variations per 10% tolerances of L , t_{Si} , and t_{ox} .

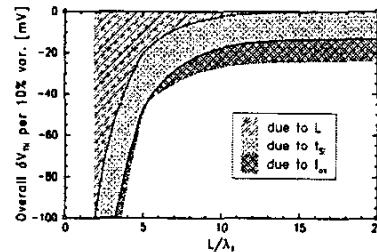


Figure 8. Decomposition of overall worst-case δV_{TH} per 10% tolerances of L , t_{Si} , and t_{ox} in ADG.

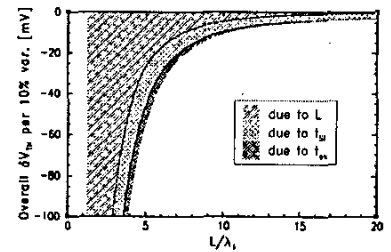


Figure 9. Decomposition of overall worst-case δV_{TH} per 10% tolerances of L , t_{Si} , and t_{ox} in SDG (after [1]).

