

Table I. Both have metal 3 connected in series with metal 2 and metal 2 connected in parallel with metal 1, to reduce the resistance of the device.

On-wafer testing was performed with the *HP-8719ES* Network Analyzer and *Cascade Microtech ACP 40* ground–signal–ground (GSG) probes. The measurement system was calibrated using the SOLT technique between 500 MHz–8 GHz with an ISS substrate standard from *Cascade*. The four step de-embedding process [7] was used to de-embed the influence of the test fixture in the measurement. The results from the measurements are shown in Table II. The obtained Q are quite good for such values of inductance, using series connected multilevel inductors in a CMOS process.

IV. CONCLUSIONS

In this brief, a new geometry for circular series connected multilevel integrated spirals is presented. The better performance of this geometry is based on the higher overlapping between layers than in the conventional geometry. This maximizes the shared flux and so the inductance, becoming a more effective inductor in terms of inductance. This assumption has been proven using a 3-D electromagnetic solver. In conclusion, two inductors were laid out using this geometry in a 0.6 μm 3 metal CMOS process.

REFERENCES

- [1] J. Craninx and M. Steyaert, *Wireless CMOS Frequency Synthesizer Design*. Norwell, MA: Kluwer, 1998.
- [2] Y. Hong and M. Frei, "An approach for fabricating high-performance inductors on low-resistivity substrate," *IEEE J. Solid State Circuits*, vol. 33, pp. 1433–1438, Sept. 1998.
- [3] A. M. Niknejad, "Analysis, design and optimization of spiral inductors and transformers for Si RF ICs," M.Phil. Elect. Eng. thesis, Univ. California, Berkeley, CA.
- [4] J. N. Burghartz, K. A. Jenkins, and M. Soyuer, "Multilevel-spiral inductors using VLSI interconnect technology," *IEEE Electron Device Lett.*, vol. 17, pp. 428–430, Sept. 1996.
- [5] M. Geen, R. Green, R. G. Arnold, and J. A. Jenkins, "Miniature multilayer spiral inductors for GAAS MMICs," in *11th Annual GaAs IC Symp.*, vol. 23, July–Aug. 1995, pp. 381–394.
- [6] J. Aguilera, "A guide for on-chip inductor design in a conventional CMOS process for RF applications," *Appl. Microw. Wireless*, pp. 56–65, Oct. 2001.
- [7] T. Kolding, "On-wafer calibration techniques for giga-hertz CMOS measurements," in *Proc. IEEE Int. Conf. on Microelectronic Test Structures*, vol. 12, Mar. 1999, pp. 105–110.

A Comprehensive Analytical Subthreshold Swing (S) Model for Double-Gate MOSFETs

Qiang Chen, Bhavna Agrawal, and James D. Meindl

Abstract—A general analytical subthreshold swing (S) model for symmetric DG MOSFETs is derived using evanescent-mode analysis. Through a concept of effective conducting path, it explains a unique doping concentration (N_A) dependence of S , providing a unified understanding of previous S models and leading to a new improved S model for undoped DG MOSFETs. Compact, explicit expressions of a scale length are derived, which expedite projections of scalability of DG MOSFETs and its requirement.

Index Terms—Double-gate MOSFET, MOSFETs, scale length, scaling, subthreshold swing, undoped.

I. INTRODUCTION

THE DOUBLE-GATE (DG) MOSFET shown in Fig. 1 has been proposed as a viable option for extending CMOS scalability beyond 50 nm partly due to its ideal subthreshold swing (S) [1]–[4]. While the majority of research has focused on numerical simulations, an analytical S model is desired to gain physical insights. A previous S model by Agrawal *et al.* was developed assuming the subthreshold current flows at the Si/SiO₂ surfaces as in bulk devices [5]. However, Tosaka *et al.* proposed an S model [6] based on an observation from simulations that "the punchthrough current dominantly flows at the SOI center," but no explanations were provided. On the other hand, the parabolic potential approximation used in [6] has been shown inaccurate and inferior to evanescent-mode analysis [7]. Moreover, it is found that agreement between both previous S models and numerical simulations remains to be improved. This paper solves the two-dimensional (2-D) Poisson equation in the channel region using evanescent-mode analysis to derive a general S model that agrees well with Medici simulations. Through a concept of effective conducting path, the model explains a unique N_A -dependence of S in DG MOSFETs, providing a unified understanding of previous S models and leading to a new improved S model for undoped DG MOSFETs. As typical of evanescent-mode analysis, a scale length is derived and its explicit expressions are provided that expedite projections of scalability of DG MOSFETs.

II. MODELS AND DISCUSSIONS

Under the full depletion condition, the subthreshold channel potential (Ψ) is approximately described by the 2-D Poisson equation $\nabla^2 \Psi = qN_A/\epsilon_{\text{Si}}$, where q is the electronic charge and ϵ_{Si} is the silicon permittivity. Using the superposition method [5], Ψ is calculated as $\Psi(x, y) = V_{GS} - \Phi_{MS} + U_{1D}(y) + \phi_{2D}(x, y)$, where V_{GS} is the gate voltage and Φ_{MS} is the gate-channel work function difference,

$$U_{1D}(y) = \frac{V_A}{2} \left(\frac{y^2}{t_{\text{Si}}^2} - \frac{1}{4} - \frac{1}{r} \right).$$

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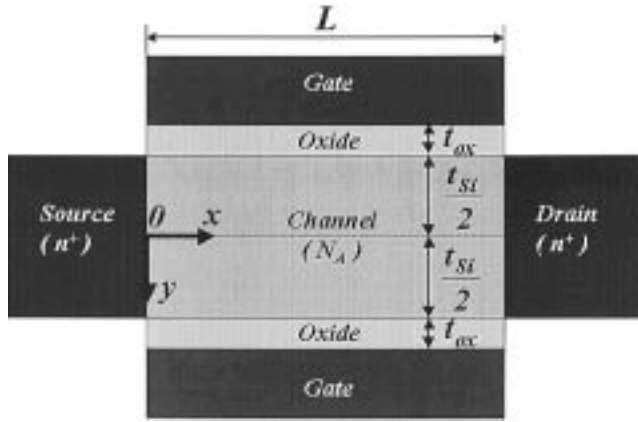


Fig. 1. Symmetric DG MOSFET with a coordinate system. $y = \pm(t_{Si}/2)$ and $y = 0$ correspond to Si/SiO₂ interfaces and the channel center, respectively.

t_{Si} is the channel thickness, $V_A = qN_A t_{Si}^2 / \epsilon_{Si}$ and measures significance of the dopant-induced field, $r = \epsilon_{ox} t_{Si} / \epsilon_{Si} t_{ox}$, t_{ox} is the gate-oxide thickness, and ϵ_{ox} is the oxide permittivity. The terms of $V_{GS} - \Phi_{MS} + U_{1D}(y)$ represent the solution to the one-dimensional (1-D) Poisson equation in the vertical direction, describing how ionized dopant atoms define the channel potential in a long channel device. $\phi_{2D}(x, y)$ is a solution to the 2-D Laplace equation, describing the impact of the source/drain. Satisfying boundary conditions at all four sides and, in particular

$$\frac{\epsilon_{ox}}{t_{ox}} \phi_{2D} \left(x, \mp \frac{t_{Si}}{2} \right) = \pm \epsilon_{Si} \frac{\partial \phi_{2D}(x, y)}{\partial y} \Big|_{y=\mp(t_{Si}/2)}$$

at the top and bottom Si/SiO₂ interfaces as required by continuity of the normal component of electric displacement and continuity of potential, ϕ_{2D} is found as follows:

$$\phi_{2D}(x, y) = \sum_j \Gamma_j \cos \frac{y}{\lambda_j} \left[V_j \left(\sinh \frac{x}{\lambda_j} + \sinh \frac{L-x}{\lambda_j} \right) + V_{DS} \sinh \frac{x}{\lambda_j} \right] / \sinh \frac{L}{\lambda_j} \quad (1)$$

where λ_j s are eigenvalues satisfying

$$\begin{aligned} \tan \frac{t_{Si}}{2\lambda_j} &= \frac{r\lambda_j}{t_{Si}}, \\ \Gamma_j &= \frac{2\lambda_j}{t_{Si}} \sqrt{1 + \frac{t_{Si}^2}{r^2\lambda_j^2}} / \left(\frac{1}{r} + \frac{1}{2} + \frac{1}{2} \frac{t_{Si}^2}{r^2\lambda_j^2} \right), \\ V_j &= V_{bi} - V_{GS} + \Phi_{MS} + V_A \lambda_j^2 / t_{Si}^2. \end{aligned}$$

V_{bi} is the junction built-in voltage and V_{DS} is the drain voltage. Exploiting the prominence of the lowest-order mode (i.e., $j = 1$) in series summation (1) [5], [7], [8] and assuming $\exp(-L/\lambda_1) \ll 1$ [5], [6], the minimum channel potential $\Psi_{min}(y)$ (i.e., “virtual cathode”) can be found through $\partial\Psi(x, y)/\partial x = 0$ as

$$\Psi_{min}(y) \approx V_{GS} - \Phi_{MS} + U_{1D}(y) + 2\Gamma_1 \cdot \cos \frac{y}{\lambda_1} \sqrt{V_1(V_1 + V_{DS})} e^{-(L/2\lambda_1)}. \quad (2)$$

Assuming that the drain current (I_D) is proportional to the total amount of free electrons at the virtual cathode and their density $n_m(y)$ follows the classic Boltzmann distribution as $n_m(y) = (n_i^2/N_A) e^{q\Psi_{min}/kT}$, where n_i is the intrinsic electron density, k is Boltzmann constant and T is temperature, a general S model is obtained as

$$\begin{aligned} S &= \frac{\partial V_{GS}}{\partial \log I_D} \\ &= \left[1 - 2\Gamma_1 \frac{(V_1 + V_{DS}/2)}{\sqrt{V_1(V_1 + V_{DS})}} \cos \frac{d_{eff}}{\lambda_1} e^{-(L/2\lambda_1)} \right]^{-1} \\ &\quad \cdot \frac{kT}{q} \ln 10 \end{aligned} \quad (3)$$

where the parameter d_{eff} is defined such that

$$\cos \frac{d_{eff}}{\lambda_1} = \frac{\int_{y=0}^{t_{Si}/2} \cos \frac{y}{\lambda_1} n_m(y) dy}{\int_{y=0}^{t_{Si}/2} n_m(y) dy}. \quad (4)$$

Thus, d_{eff} represents the location of an S -wise weighted “center of gravity” of subthreshold conduction (or “effective conducting path”) with its value determined by the shape of $n_m(y)$ or potential profile $\Psi_{min}(y)$.

The general S model is compared to Medici simulations as well as to previous S models in Fig. 2(a), revealing an unusual N_A -dependence of S , which is opposite to that in bulk devices. Increasing N_A does not compromise, but improves S in DG MOSFETs within the full depletion range. Such a dependence can be explained by the location of effective conducting path d_{eff} , as illustrated in Fig. 2(b). For high N_A values, the dopant induced field $U_{1D}(y)$ is significant (for $N_A = 5 * 10^{18} \text{ cm}^{-3}$ and $t_{Si} = 20 \text{ nm}$, $V_A \approx 3 \text{ V}$) such that the surface potential $\Psi_{min}(y = \pm t_{Si}/2)$ is much greater than the center potential $\Psi_{min}(y = 0)$ and the overall conduction is highly confined to surfaces. Consequently, the effective conducting path is found at surfaces (i.e., $d_{eff} = t_{Si}/2$), subject to immediate gate control, resulting in an improved S . The S model in [5] can actually be obtained from the general S model (3) by substituting $d_{eff} = t_{Si}/2$. With decreasing N_A values, a weakened dopant-induced field $U_{1D}(y)$ leads to a flatter shape of potential profile such that the effective conducting path retreats from surfaces into depth (i.e., $d_{eff} < t_{Si}/2$), causing weakened gate control and a larger S . Finally, $U_{1D}(y)$ becomes negligible at low N_A values (for $N_A = 10^{16} \text{ cm}^{-3}$ and $t_{Si} = 20 \text{ nm}$, $V_A \approx 6 \text{ mV}$) and the potential profile is virtually determined by 2-D effects ϕ_{2D} alone. Consequently, the effective conducting path no longer drifts with N_A , resulting in a constant S value.

In undoped (or lightly doped with $N_A \leq 10^{16} \text{ cm}^{-3}$ [10]) DG MOSFETs, the channel potential, being determined by 2-D effects ϕ_{2D} alone, is greater at channel center ($y = 0$) than at surfaces ($y = \pm t_{Si}/2$) [see (2)], making channel center more leaky than anywhere else, as first observed in [11]. However, the difference between surface and center potentials is quite limited because of the 2-D nature of its formation and significantly less (in absolute value) than that in heavily doped cases. Due to this relatively even spreading of free electrons, the overall conduction is not confined to the channel center and the effective conducting path should be somewhere in-between surfaces and channel center as illustrated in Fig. 2(b). As a first-order approximation, $d_{eff} = t_{Si}/4$. In Fig. 3, an undoped S model, obtained by substituting $d_{eff} = t_{Si}/4$ into (3), is verified with Medici simulations and compared to the model of Tosaka *et al.* and a center S model obtained by substituting $d_{eff} = 0$ into (3). It is interesting to notice that the latter two models, although derived from different approaches but both

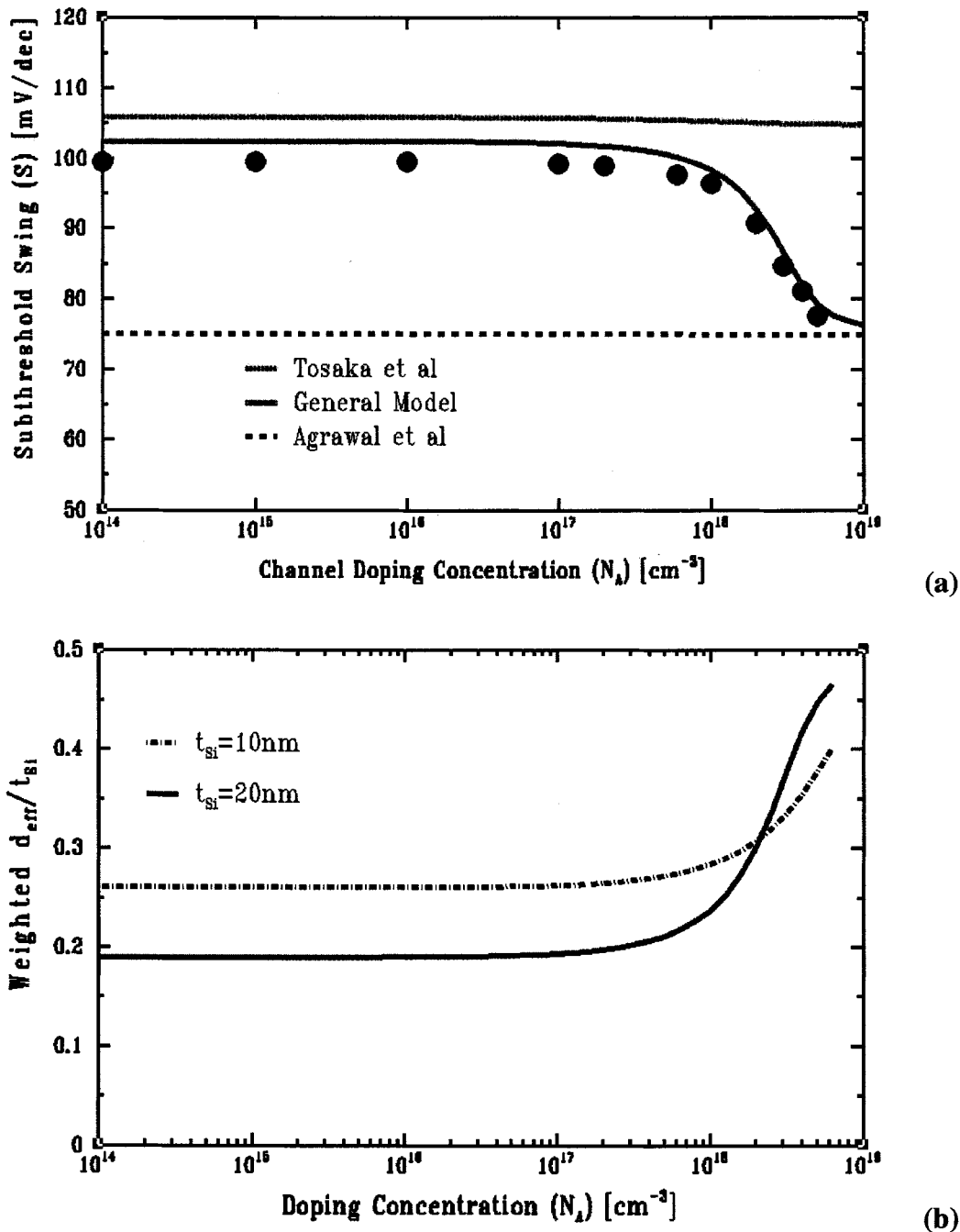


Fig. 2. Doping concentration (N_A) dependence of S and its explanation. (a) Comparison of general S model with previous S models ($L = 30$ nm, $t_{ox} = 1.5$ nm, $t_{Si} = 20$ nm, and $V_{DS} = 0.1$ V). Symbols are Medici simulations. (b) N_A -dependence of the location of effective conducting path (d_{eff} , normalized to channel thickness t_{Si}) ($L = 30$ nm, $t_{ox} = 1.5$ nm).

assuming *exclusive* center conduction, are very close to one another, while the newly proposed undoped S model demonstrates improved agreement with simulations.

It is worthwhile to point out that the S value resulting from surface conduction, although being improved compared to undoped cases as shown in Fig. 2(a), may not be achievable in aggressively scaled devices because, with ever decreasing silicon thickness, it requires higher and higher doping level to obtain surface conduction mode as illustrated in Fig. 2(b), which may cause a band-to-band tunneling problem.

One key physical effect neglected in the analysis of this paper is quantum effects of both field confinement and spatial confinement. In heavily doped devices, field confinement in the inversion layer caused

by strong electric field shifts electron peaks away from surfaces [12], which constitutes one more reason for inaccuracy of a surface S model. On the other hand, undoped devices inherently have free electrons quite evenly spreading the whole silicon layer resulting in a small vertical electric field. Therefore, field confinement in undoped DG MOSFET is negligible in the subthreshold region and does not have an effect on S . Spatial confinement becomes significant when t_{Si} drops much below 5 nm [2] where carrier distribution must be found from Schrodinger and Poisson equations self-consistently. Thus, the undoped S model is expected to hold for t_{Si} not much less than 5 nm.

As in previous scaling studies, [8], [13], analytical expressions are highly desired for the scale length: the lowest-order eigenvalue λ_1 .

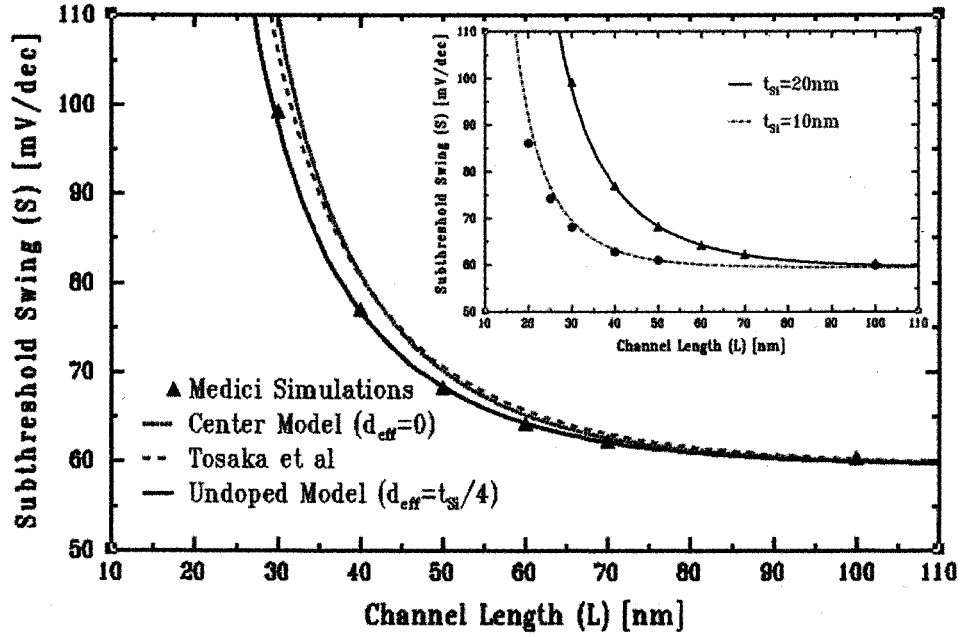


Fig. 3. Verification of undoped S model ($N_A = 10^{16} \text{ cm}^{-3}$, $t_{ox} = 1.5 \text{ nm}$, $t_{Si} = 20 \text{ nm}$, and $V_{DS} = 0.1 \text{ V}$). The inset compares undoped S model with Medici simulations for two different values of silicon thickness ($N_A = 10^{16} \text{ cm}^{-3}$, $t_{ox} = 1.5 \text{ nm}$, and $V_{DS} = 0.1 \text{ V}$. Symbols are Medici simulations).

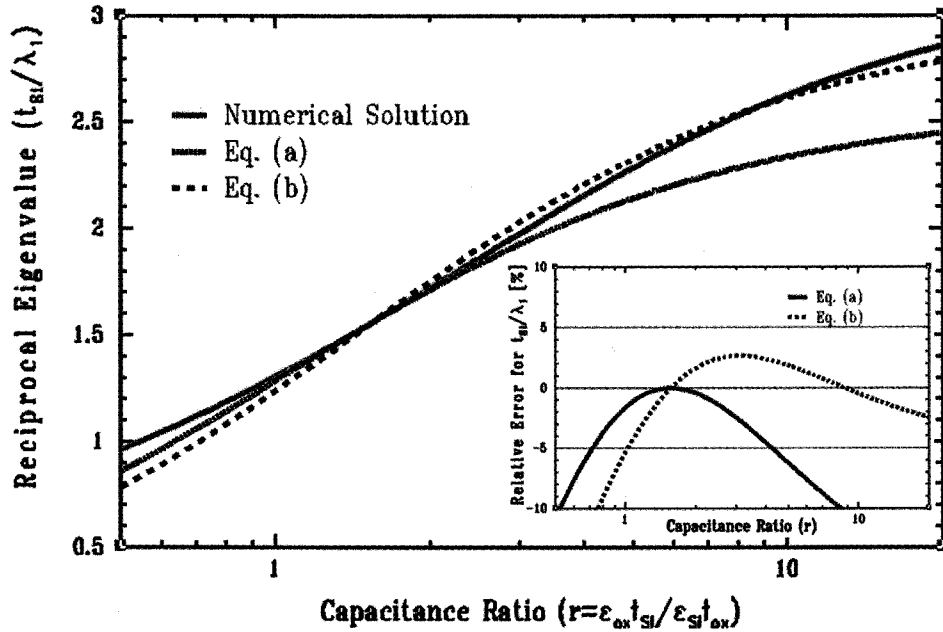


Fig. 4. Comparison of approximate expressions of λ_1 with exact numerical solution. The inset shows the relative error of approximate expressions in percentage.

Being a solution to a transcendental equation, λ_1 in general cannot be found explicitly. However, approximate expressions are possible

$$\begin{aligned} \text{a) } \lambda_1 &= \frac{1 + 1/r}{1 + \pi/2} t_{Si} = \frac{t_{Si} + \epsilon_{Si} t_{ox} / \epsilon_{ox}}{1 + \pi/2} \\ \text{b) } \lambda_1 &= \frac{1 + \sqrt{2}/r}{\sqrt{2} + \pi/2} t_{Si} = \frac{t_{Si} + \sqrt{2} \epsilon_{Si} t_{ox} / \epsilon_{ox}}{\sqrt{2} + \pi/2} \end{aligned} \quad (5)$$

for $r \leq \pi/2$ and $r > \pi/2$, respectively, and are compared to the exact numerical solution of λ_1 in Fig. 4. For a practical range of r values from 0.8 to 20 (it corresponds, for example, to t_{Si} from 3.6 nm to 91

nm for $t_{ox} = 1.5 \text{ nm}$), the relative error of (5) is less than 3%, which seems reasonable for scaling study purposes. Using (5) and a simplified version of the undoped S model

$$S = \left(1 - 2\Gamma_1 \cos \frac{t_{Si}}{4\lambda_1} e^{-(L/2\lambda_1)} \right)^{-1} \frac{kT}{q} \ln 10 \quad (6)$$

design contours of a 15-nm undoped symmetric DG MOSFET are presented in Fig. 5(a) for different S requirements. It seems extremely challenging to meet the low power requirement for $S = 70 \text{ mV/dec}$ already at the 15 nm generation. Scaling capability of the undoped DG MOSFET is further illustrated in Fig. 5(b), where the minimum channel length versus t_{Si} is projected for $S = 100 \text{ mV/dec}$ and $S = 70 \text{ mV/dec}$

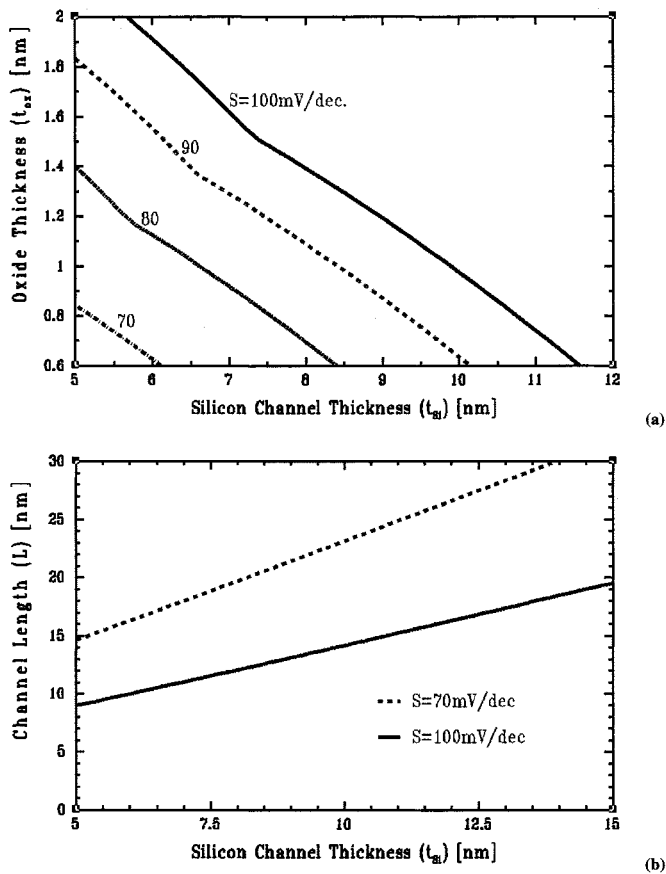


Fig. 5. Scaling capability of DG MOSFETs. (a) Design contours of a 15-nm undoped DG MOSFETs for different S requirements. (b) Projections of minimum channel length as a function of silicon thickness (t_{ox} is assumed to be 0.8 nm).

(t_{ox} is assumed to be 0.8 nm). Clearly, 10 nm undoped DG MOSFETs are likely to find their first applications in places where $S = 100$ mV/dec is tolerable.

III. CONCLUSIONS

A general analytical S model for symmetric DG MOSFETs is derived using evanescent-mode analysis. Through a concept of effective conducting path, the model explains a unique N_A dependence of S , providing a unified understanding of previous S models and leading to a new improved S model for undoped DG MOSFETs. Compact, explicit expressions of a scale length are derived that expedite projections of scalability of DG MOSFETs and its requirement.

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REFERENCES

- [1] D. J. Frank, S. E. Laux, and M. V. Fischetti, "Monte Carlo simulation of a 30 nm dual-gate MOSFET: How short can Si go?," in *IEDM Tech. Dig.*, 1992, pp. 553–556.
- [2] H.-S. P. Wong, D. J. Frank, and P. M. Solomon, "Device design consideration for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFETs at the 25 nm channel length generation," in *IEDM Tech. Dig.*, 1998, pp. 407–410.
- [3] Z. Ren, R. Venugopal, S. Datta, M. Lundstrom, D. Jovanovic, and J. Fossum, "The ballistic nanotransistor: A simulation study," in *IEDM Tech. Dig.*, 2000, pp. 715–718.

- [4] J. G. Fossum, "Physical insights on double-gate MOSFETs," in *Proc. Dig. Government Microcircuit Appl. Conf.*, Mar. 2001, pp. 322–325.
- [5] B. Agrawal, "Comparative scaling opportunities of MOSFET structures for gigascale integration (GSI)," Ph.D. dissertation, Rensselaer Polytech. Inst., Troy, NY, 1994.
- [6] Y. Tosaka, K. Suzuki, and T. Sugii, "Scaling-parameter-dependent model for subthreshold swing S in double-gate SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 15, pp. 466–468, Nov. 1994.
- [7] S.-H. Oh, D. Monroe, and J. M. Hergenrother, "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 21, pp. 397–399, Sept. 2000.
- [8] D. J. Frank, Y. Taur, and H.-S. P. Wong, "Generalized scale length for two-dimensional effects in MOSFETs," *IEEE Electron Device Lett.*, vol. 19, pp. 385–387, Oct. 1998.
- [9] Y. Taur, "An analytical solution to a double-gate MOSFET with undoped body," *IEEE Electron Device Lett.*, vol. 21, pp. 245–247, May 2000.
- [10] —, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 48, pp. 2861–2869, Dec. 2001.
- [11] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 40, pp. 2326–2329, Dec. 1993.
- [12] M. Shoji and S. Horiguchi, "Electronic structures and phonon-limited electron mobility of double-gate silicon-on-insulator Si inversion layers," *J. Appl. Phys.*, vol. 85, pp. 2722–2731, Mar. 1999.
- [13] D. Monroe and J. M. Hergenrother, "Evanescent-mode analysis of short-channel effects in fully depleted SOI and related MOSFETs," in *Proc. IEEE SOI Conf.*, Oct. 1998, pp. 157–158.

Effect of Reverse Biased Voltage at Source and Drain on Plasma Damage

Durga Misra

Abstract—We have examined the possible effects of reverse-biased floating potential at the source and drain during plasma processing on the performance of n-channel metal–oxide–semiconductor field-effect transistors (MOSFETs). Threshold voltage degradation was evaluated by subjecting the gate oxide to high-field injection. Device degradation is found to be enhanced with the floating potential at source and drain for the devices subjected to substrate injection. An increase in electron trapping was observed with an increase in floating potential. Estimation shows that the effective antenna ratio of MOSFET increases with the reverse-biased floating voltage at source and drain. Our results indicate that plasma-charging damage can be significant even under uniform plasma if a potential is developed at the antenna-connected source and drain terminals. Damage in devices subjected to gate injection on the other hand, could have minimal dependence on source and drain potential.

Index Terms—Current stress, effective antenna ratio, plasma damage.

I. INTRODUCTION

Plasma-induced wafer charging is a serious problem in plasma processing. Thin gate oxide in metal–oxide–semiconductor (MOS) transistor is damaged during plasma processing due to high-field electron

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