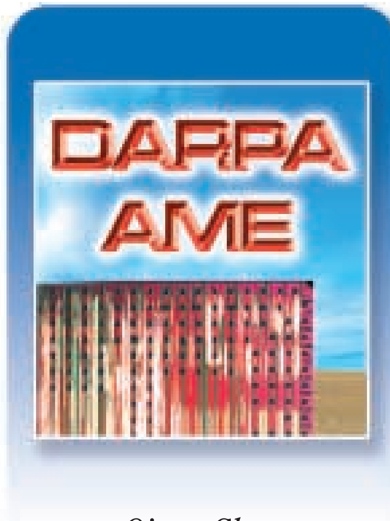
DOUBLE JEOPARDY IN THE NANOSCALE COURT?

Modeling the Scaling Limits of Double-Gate MOSFETs with Physics-Based Compact Short-Channel Models of Threshold Voltage and Subthreshold Swing



Qiang Chen, Keith A. Bowman, Evans M. Harrell, and James D. Meindl

Over the past three decades, the primary driver of the exponential improvements in integrated circuit performance has been the scaling of MOSFET dimensions. The double-gate silicon-on-insulator (DG SOI) MOSFET structure is widely expected to extend MOSFET scaling to and beyond the 65 nm technology node with physical gate lengths below 25 nm [1]. The superior scalability of this novel device has been demonstrated by previous studies [2]-[9]. While the majority of these analyses are based on numerical simulations, which provide accurate results, physical, compact, analytical device models are highly desired. In this article, such models of threshold voltage and subthreshold swing for undoped symmetric DG SOI MOSFETs are presented. These models are used to reveal physical insights into device operating principles, to provide efficient guidelines for device designs, and to enable a comprehensive projection of scaling limits and opportunities of DG SOI MOSFETs.

Short-Channel Effects and DG SOI MOSFETs

Two key characteristics of a MOSFET are the threshold voltage (V_{TH}) and the subthreshold swing (S). The threshold voltage is the value of the gate voltage that turns on the transistor by inducing a highly conductive channel from the source to the drain. The subthreshold swing is the gate voltage change that is required for an order-of-magnitude change of the drain current in the subthreshold region. As the channel length (L) of a typical MOSFET is reduced with all other parameters held constant, the threshold voltage decreases and the subthreshold swing increases, as illustrated in Figure 1. Collectively, threshold voltage rolloff and subthreshold swing rollup are commonly known as short-channel effects (SCEs). In consequence of SCEs, the ratio of the drive (ON) current to the leakage (OFF) current is substantially reduced, which imposes severe tradeoffs between circuit speed and standby power. In addition, SCEs amplify the impact of process variations on CMOS circuits.

In conventional bulk MOSFETs, SCEs are caused by the lateral electric fields from the source to channel and drain to channel. As L decreases, the lateral fields terminate on more charge further into the channel, which essentially steals the charge that would normally be terminated by the gate voltage in a long-channel device. This stealing of charge by the lateral fields effectively lowers the source-to-channel barrier, which controls the conduction of electrons from source to drain. To limit this charge stealing, and thus mitigate SCEs, heavy channel doping is exploited in bulk MOSFETs. As the gate length is scaled to 50 nm and below, the required channel doping concentration is expected to be a few times 10^{18} cm^{-3} and above [10]. These extremely high doping levels, however, lead to 1) severe degradation of the carrier mobility as the impurity

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scattering becomes dominant [10] and 2) severe threshold voltage variations due to random microscopic fluctuations of dopant atoms [11].

The DG MOSFET, as illustrated in Figure 2, does not require channel doping for SCE control. Instead, this novel device uses a second gate and a fully depleted silicon film as the channel to enhance the electrostatic control of the gates over the channel, which effectively suppresses the impact of the source/drain. The thin silicon film is undoped or lightly doped (typical doping concentration N_A<10^{16} cm^{-3} [12]) to guarantee the full depletion condition. For the most effective SCE control, the two gate-oxide layers are equally thin. Use of an identical material for both gates results in a symmetric DG MOSFET.

The DARPA Advanced Microelectronics Program

In 1997, the Defense Advanced Research Projects Agency (DARPA) initiated a research program to explore the limits of scaled transistors and integration. That research program, the DARPA Advanced Microelectronics (AME) Program, was based on several prior DARPA programs, including the ULTRA Program that had been exploring nano-scale nonsilicon devices and the Low Power Program that had been developing silicon-on-insulator technologies, as well several other technological advances of the time. The first DARPA Program Manager for the program was Dr. Fabian Pease. On Fabian's return to Stanford University around 1998, I inherited the program and managed its midcourse and completion. The overall goals of the AME Program were to explore the future of microelectronics far beyond the end of the technology roadmap that existed at the time. Within the program itself, the objectives were to explore the technologies for creating useful devices with minimum channel dimensions of 25 nm, potential scales of integration approaching 1E12 transistors per chip (terascale integration), with room-temperature operation. At the outset of the program, about a dozen research contracts with leading-edge companies, universities, and other organizations were funded and three technological areas were identified as being crucial:

- 1) active devices suitable for terascale integration (e.g., with overall dimensions less than 150 nm squared, transconductance >100 S/m, power delay products approaching 10aJ)
- 2) monolithic structures with many layers of high-quality active devices (3-D integration)
- 3) interconnect strategies.

The major emphasis of the AME program was on exploring candidate scaled devices for terascale integration applications (areas 1 and 2). The interconnects for advanced devices and circuits received less attention by comparison but has certainly been (and is being) addressed by other research programs and by the industry.

The program has been completed and was extremely successful. The scientists and engineers in the program pursued many novel and innovative devices. Some of those candidate devices were innovations on and variations of the traditional MOSFET (i.e., the current is varied by controlling the height of a thermal barrier); vertical transistor-type devices in several configurations; and other switching devices that relied on controlling the channel current through modulation of various forms of tunneling barriers. Opportunities to impact future circuit architectures and to solve interconnection issues were explored through work on 3-D fabrication. Clever approaches were worked on, but those technologies were taken up comparatively late in the program and remain rather speculative. The articles in this issue describe the device and related technology work that is representative of what was undertaken and accomplished in the program.

Daniel J. Radack
DARPA/MTO

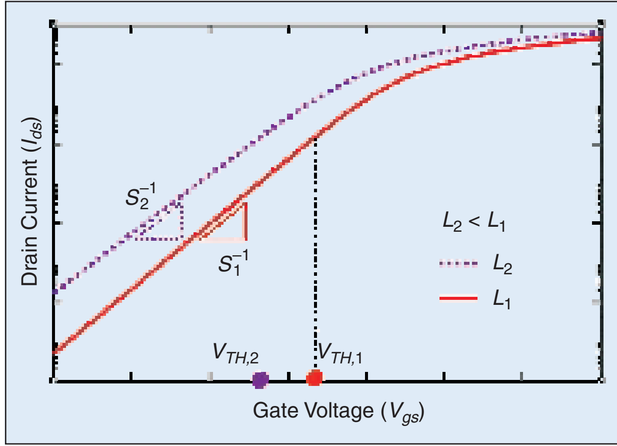
Subthreshold Swing Model

The superb turn-off characteristic of undoped DG MOSFETs can be comprehended through the gate-to-gate capacitive coupling. For large channel lengths, the impact of the source/drain can be ignored, and the channel potential is modulated by the gate voltage only. Since the thin silicon film is fully depleted and the amount of mobile charges in the subthreshold region is negligible, the silicon film behaves like a dielectric with respect to the gates, which is analogous to a dielectric layer of a capacitor with respect to its two plates. As the voltage on both gates swings *in sync*, any change in gate voltage induces the same amount of potential change everywhere in the channel. Such a one-to-one relationship between the gate voltage change and channel potential change exerts a perfect electrostatic control of the gate over the subthreshold leakage current, which exponentially depends on the channel potential. Therefore, the subthreshold swing of a *long*-channel undoped DG MOSFET has an ideal value and is calculated as [13]

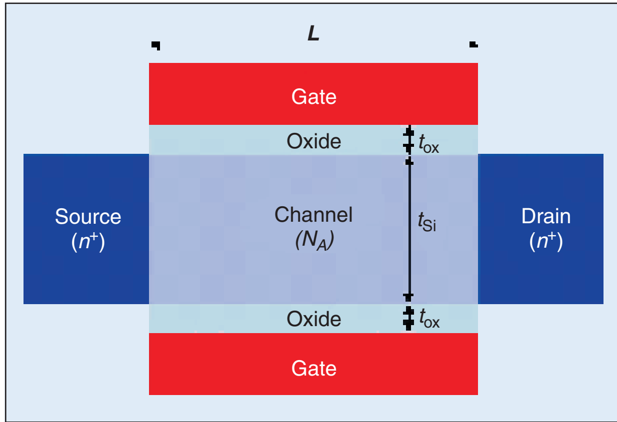
$$S = \frac{\partial V_{gs}}{\partial \log_{10} I_{ds}} = \frac{kT}{q} \ln 10, \qquad (1)$$

where V_{gs} is the gate voltage, I_{ds} is the drain current, k is the Boltzmann constant, T is the absolute temperature, and q is the electron charge. At room temperature (T=300 K) (1) gives ~60 mV/dec.

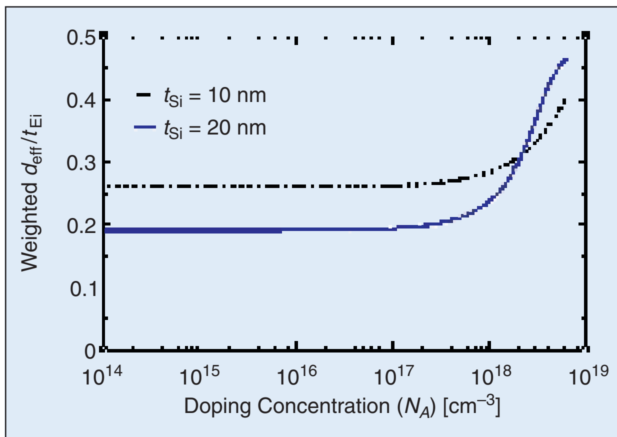
In long-channel undoped symmetric DG MOSFETs, besides the ideal value of the subthreshold swing, a unique physical phenomenon, called volume inversion [14], is observed. Since the channel region contains such a small amount of fixed ionized dopant charges, the silicon film is virtually equi-potential across the thickness. Essentially, the entire silicon film is inverted by the gate voltage to the same degree and takes part in the subthreshold leakage collectively. This volume inversion effect, as demonstrated later, is important to appropriate subthreshold and near-threshold characterization of symmetric DG MOSFETs.



1. Impact of short-channel effects on drain current. As the channel length (L) is reduced, subthreshold swing increases ($S_2 > S_1$) and threshold voltage decreases ($V_{TH,2} < V_{TH,1}$).



2. Schematic of the cross section of a symmetric double-gate MOSFET. The channel is undoped or lightly doped with the doping concentration (N_A) less than 10^{16} cm^{-3}.



3. "Center of gravity" of subthreshold leakage in each half of the silicon film, normalized to the film thickness, versus channel doping concentration. The ordinate 0 corresponds to the film center, and 0.5 corresponds to the Si/SiO$_2$ interface. L=30 nm and t_{ox} = 1.5 nm. After [15].

The subthreshold swing of a short-channel DG MOSFET is impaired by the source/drain. In the subthreshold region, the gate voltage is applied to keep the electrostatic potential of the channel sufficiently low to reduce the amount of mobile carriers in the channel and turn off the transistor. The channel potential near the source/drain, however, is pinned to the much higher potentials of the source/drain, where mobile carriers are abundant with concentrations above 10^{20} cm^{-3}. As a result, every effort of the gate voltage to lower the channel potential and turn off the transistor has to in part overcome the opposition from the source/drain potentials in a *short*-channel DG MOSFET. A degraded turn-off characteristic, corresponding to an increased subthreshold swing, results. Such a physical mechanism can be described mathematically by solving a two-dimensional Poisson equation that includes the term of fixed ionized dopant charges only [15].

The potential solution provides yet another insightful view of the SCEs and their control in the undoped symmetric DG MOSFETs. The electrostatic potential at the channel center turns out to be slightly higher than at other positions across the silicon film thickness in a short-channel device [15], and the channel center appears most leaky [16]. This results from the control of the gate voltage being most weakened by the source/drain potentials at the channel center, which is the furthest point of the channel from both gates. Consequently, to suppress the SCEs the vertical electrical distance between the gates and the channel center must be much smaller than half of the channel length; i.e.,

$$\frac{t_{Si}}{2} + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} << \frac{L}{2}, \tag{2}$$

where t_{Si} and t_{ox} are silicon channel and gate oxide thickness, respectively, and ε_{Si} and ε_{ox} are silicon and gate oxide permittivity, respectively. Both a thin silicon film and a thin gate oxide are thus required to scale undoped DG MOSFETs.

The electrostatic potential difference between the channel center and the Si/SiO$_2$ interfaces, however, is quite limited in a short-channel device because of its two-dimensional nature. The volume inversion remains in effect. Its presence is confirmed in Figure 3, which depicts the normalized position of the "center of gravity" of subthreshold leakage in each half of the silicon film. For undoped devices, this "center of gravity" lies neither at the silicon film center nor at the Si/SiO$_2$ interface but rather approximately halfway in between.

The analytical solution of the two-dimensional Poisson equation in combination with the volume inversion effect leads to a compact subthreshold swing model for undoped symmetric DG MOSFETs [15]

$$S = \left(1 - 2\Gamma_1 \cos\frac{t_{Si}}{4\lambda_1} e^{-\frac{L}{2\lambda_1}}\right)^{-1} \frac{kT}{q} \ln 10, \tag{3}$$

where the parameter Γ_1 is provided in the appendix, and λ_1 is a scale length calculated as the lowest-order solution to a transcendental equation

For large channel lengths, the impact of the source/drain can be ignored, and the channel potential is modulated by the gate voltage only.

$$\tan\frac{t_{Si}}{2\lambda_1} = \frac{r\lambda_1}{t_{Si}}, \quad (4)$$

where $r = \varepsilon_{ox} t_{Si} / \varepsilon_{Si} t_{ox}$. As shown in Figure 4, this compact subthreshold swing model agrees well with numerical Medici simulations. As the channel length is made sufficiently large, the subthreshold swing approaches its ideal value given by (1), i.e., ~60 mV/dec at room temperature. As previously discussed, a thin silicon film and a thin oxide effectively reduce the subthreshold swing rollup.

Threshold Voltage Model

Historically, the most popular definition of threshold voltage used in compact modeling is the gate voltage at which the surface electrostatic potential becomes $2\phi_B$, where ϕ_B is the difference between the Fermi level and intrinsic level of silicon in the neutral region [17]. Under this definition, the density of inverted mobile carriers at the silicon surface equals the density of the dopant atoms in the silicon bulk at the threshold voltage. This definition has been physically reasonable and successful in identifying the turn-on condition for bulk devices, where channel doping concentrations are in the range of 10^{16} cm^{-3} and higher. In undoped devices, however, the mobile carrier density that is required to turn on the transistor far exceeds the channel doping concentration [18], and the $2\phi_B$ surface potential definition no longer serves as an indicator of the turn-on condition. An alternative way of defining the threshold voltage can be adopted that uses the gate voltage when the inversion carrier *sheet* density (i.e., *integrated* inversion carrier density) reaches a constant value (Q_{TH}), which is selected to adequately reflect the turn-on condition. Such a definition is a close equivalent to the constant-drain-current measurement that is widely used in both experiments and numerical simulations [3], [7].

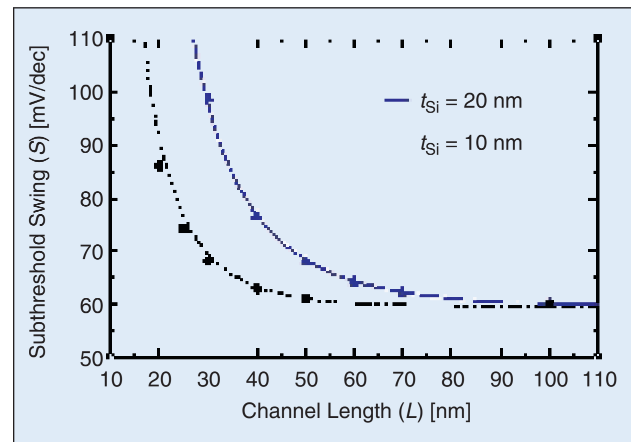
In undoped symmetric DG MOSFETs, the volume inversion remains in effect through the near-threshold region. Consequently, the electrostatics in the entire channel is determined by mobile charges, rather than by fixed ionized dopant charges, under the threshold condition. A threshold voltage model is thus derived by analytically solving the two-dimensional Poisson equation with only the mobile charge term included in the channel region [19]

$$V_{TH} = \Phi_{MS,i} + \eta\frac{kT}{q}\frac{\cosh(\theta)}{\cosh(\theta/2)}\ln\left(\frac{Q_{TH}}{n_i t_{Si}}\right) - \left[\frac{\cosh(\theta)}{\cosh(\theta/2)}\eta - 1\right]\varphi_{0m}, \quad (5)$$

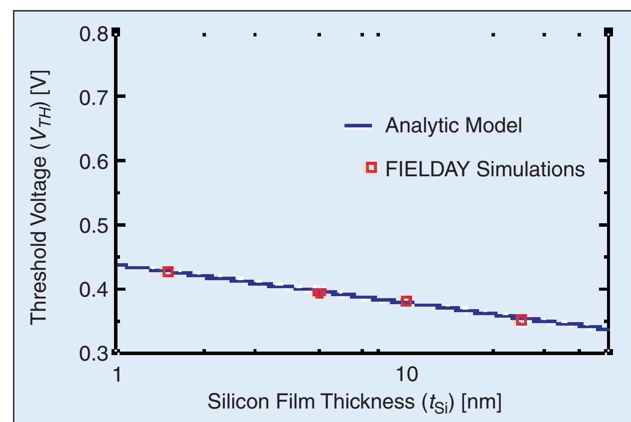
where $\Phi_{MS,i}$ is the gate workfunction referenced to intrinsic silicon and n_i is the intrinsic density of electrons. The parameters η, θ, and φ_{0m} are provided in the appendix. For sufficiently large channel lengths, (5) simplifies to a long-channel threshold voltage model

$$V_{TH,\mathrm{long}} = \Phi_{MS,i} + \frac{kT}{q}\ln\frac{Q_{TH}}{n_i t_{Si}}, \quad (6)$$

which is compared to numerical FIELDAY simulations [7] with close agreement as demonstrated in Figure 5. The constant slope of $V_{TH,\mathrm{long}}$ versus t_{Si} (in log scale) confirms the presence of the volume inversion effect. The threshold voltage rolloff (ΔV_{TH}), defined as the difference between the short-channel and



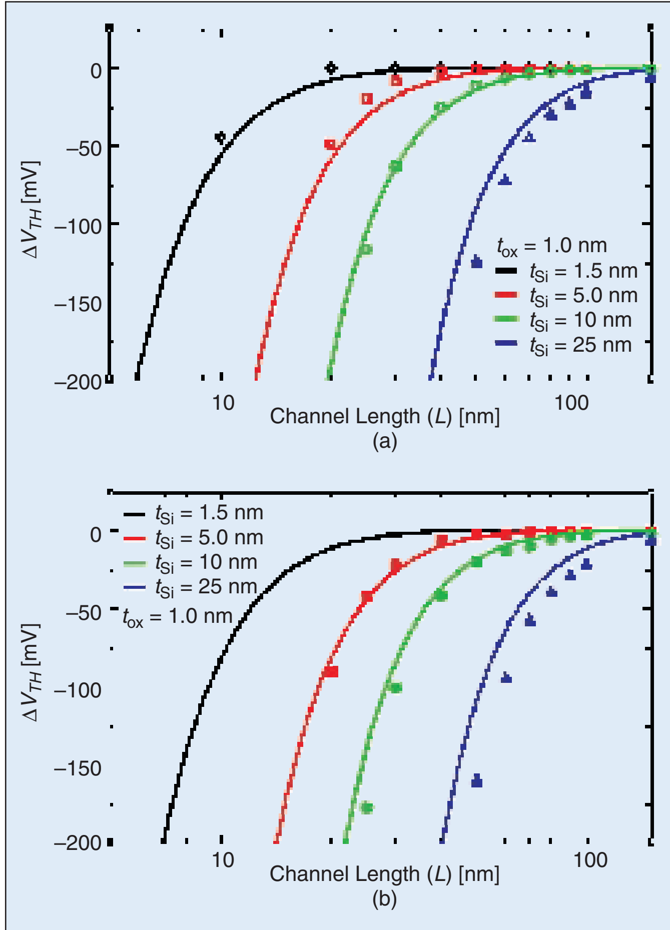
4. *Subthreshold swing versus channel length: comparison of model projections (lines) with Medici numerical simulations (discrete points) (t_{ox} = 1.5 nm). After [15].*



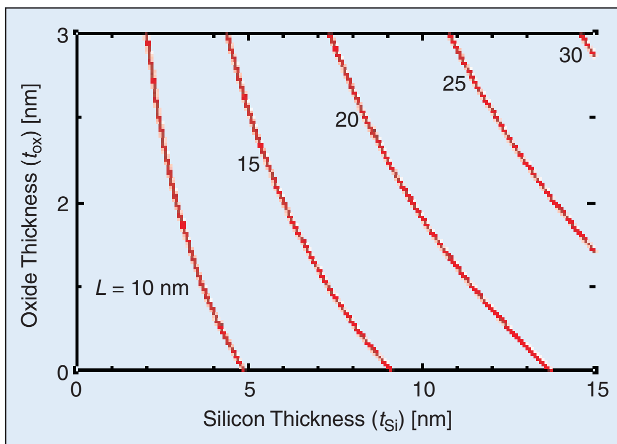
5. *Long-channel threshold voltage versus silicon film thickness: comparison of model projections (solid line) with FIELDAY numerical simulations (discrete points) [7]. After [19].*

long-channel values of threshold voltage, is then obtained from (5) and (6) as

$$\Delta V_{TH} = \left(\frac{kT}{q}\ln\frac{Q_{TH}}{n_i t_{\mathrm{Si}}} - \varphi_{0m}\right)\left[\eta\frac{\cosh\theta}{\cosh(\theta/2)} - 1\right]. \tag{7}$$



6. Threshold voltage rolloff: comparison of model projections (solid lines) with FIELDAY numerical simulations (discrete points) [7]. (a) t_{ox} = 1.0 nm. (b) t_{ox} = 1.5 nm. After [19].



7. Design contours of t_{ox} versus t_{Si} for L = 10, 15, 20, 25, and 30 nm with S = 100 mV/dec.

The rolloff model is compared to numerical FIELDAY simulations [7] with good agreement as indicated in Figure 6. A thin silicon film and a thin gate oxide are required to limit threshold voltage rolloff to acceptable levels.

Scaling Limits

As previously discussed in the subthreshold swing and threshold voltage modeling sections, a thin silicon film and a thin gate oxide are needed to suppress SCEs and to enable channel length scaling of undoped DG MOSFETs. The underlying physical explanation has been qualitatively provided above. A quantitative guideline can be obtained by studying the scale length λ_1, which characterizes the two-dimensionality of the channel potential distribution. As seen in (3), a smaller λ_1 enables a smaller channel length for the same amount of subthreshold swing rollup. Therefore, reducing λ_1 is central to scaling undoped DG MOSFETs. Simplifying for two separate conditions, $r \le \pi/2$ and $r > \pi/2$, λ_1 may be approximated as [15]

$$\lambda_1 = \frac{1+1/r}{1+\pi/2}t_{\mathrm{Si}} = \frac{t_{\mathrm{Si}} + \varepsilon_{\mathrm{Si}}t_{\mathrm{ox}}/\varepsilon_{\mathrm{ox}}}{1+\pi/2}, \tag{8}$$

$$\lambda_1 = \frac{1+\sqrt{2}/r}{\sqrt{2}+\pi/2}t_{\mathrm{Si}} = \frac{t_{\mathrm{Si}} + \sqrt{2}\varepsilon_{\mathrm{Si}}t_{\mathrm{ox}}/\varepsilon_{\mathrm{ox}}}{\sqrt{2}+\pi/2}, \tag{9}$$

respectively. Expressions (8) and (9) readily quantify the need of reducing the vertical dimension for SCE suppression, which is qualitatively described earlier in (2). In addition, (8) and (9) provide key insight into the relative effectiveness of reducing silicon film thickness versus reducing oxide thickness toward channel-length scaling. When t_{Si} is much larger than t_{ox}, λ_1 is primarily determined by t_{Si}. In this regime, reducing t_{Si} is more effective than reducing t_{ox} for the same percentage of reduction. As t_{Si} becomes comparable to t_{ox}, reduction of t_{ox} becomes equally critical. The impact of reducing t_{Si} and t_{ox} to enable channel-length scaling is illustrated in a contour plot given in Figure 7 for a constant subthreshold swing of S=100 mV/dec.

In addition to how small t_{Si} and t_{ox} can be made, the scaling limits of undoped DG MOSFETs are also dependent upon system and circuit requirements, which are determined by the desired application [20]. For this reason, four different criteria are considered. The first two criteria are based on subthreshold swing requirements of 70 mV/dec and 100 mV/dec, which correspond to excellent and moderate transistor turn-off characteristics, respectively. The third criterion mandates that threshold voltage rolloff from its long-channel value be less than 100 mV as an acceptable amount of short-channel effects [21]. The final criterion is that the "local" threshold voltage rolloff (i.e., the change of threshold voltage from its *nominal value*) should be less than 7% of the supply voltage when the channel length is 30% off its nominal value, which is similar to the criterion set forth in [22]. This criterion takes process toler-

ances into consideration, and the 30% process tolerance is a channel-length-equivalent variation that includes both channel-length variation and silicon film thickness variation. For example, the allowable "local" threshold voltage rolloff is 70 mV for a 1 V supply voltage.

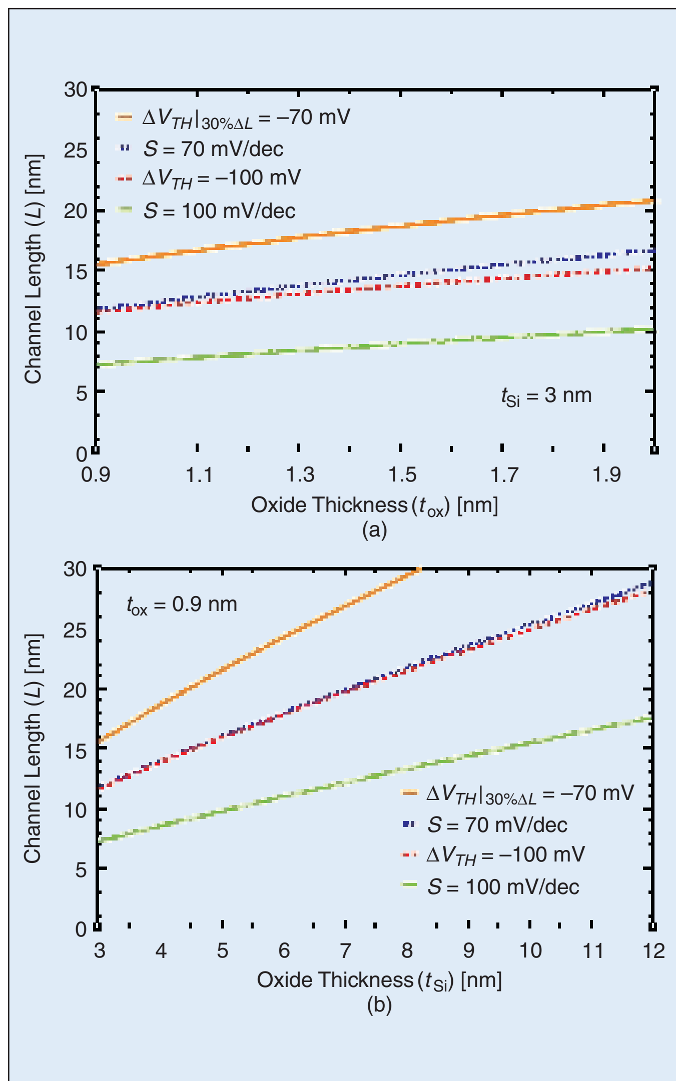
Based on these four criteria, minimum channel lengths of undoped symmetric DG MOSFETs are projected in Figure 8 as functions of $t_{\rm Si}$ and $t_{\rm ox}$. The minimum value of $t_{\rm Si}$ is assumed to be 3 nm in order to keep energy quantization effects reasonably small [7], [19]. The minimum value of $t_{\rm ox}$ (understood as the equivalent electrical oxide thickness) is set to be 0.9 nm [1]. From Figure 8, model projections indicate that the channel length of an undoped DG MOSFET as an individual device can be scaled beyond 10 nm (i.e. , ~7 nm) for a moderate turn-off behavior of S=100 mV/dec. Applying the requirement for an improved turn-off behavior of S=70 mV/dec forces the minimum channel length to increase to ~12 nm. Similar values are projected by the 100 mV "global" rolloff criterion. The most stringent limiter for scaling comes from the "local" rolloff requirement as demanded by process tolerance considerations. The model projects much larger minimum channel lengths (~16 nm) than those by all other scaling criteria. The ability to tightly control process tolerances will set the ultimate limit on scaling of undoped DG MOSFETs as a building element, rather than as an individual device, for gigascale integration.

A threshold voltage model is derived by analytically solving the two-dimensional Poisson equation with only the mobile charge term included in the channel region.

Summary/Conclusions

Physics-based compact short-channel models of threshold voltage and subthreshold swing for undoped symmetric double-gate MOSFETs were presented, which were developed from analytical solutions of the two-dimensional Poisson equations in the channel region. These models, which are in close agreement with numerical simulations, accurately characterize the subthreshold and near-threshold regions of operation by appropriately including essential phenomena such as volume inversion and the dominance of mobile charges over fixed charges under threshold conditions. Explicit, analytical expressions are derived for a scale length, which results from an evanescent-mode analysis. These equations readily quantify the impact of silicon film thickness and gate oxide thickness on the minimum channel length and device characteristics and can be used as an efficient guideline for device designs.

These newly developed models are exploited to make a comprehensive projection on the scaling limits of undoped double-gate MOSFETs. This novel device has intrinsically superb turn-off characteristics and superior short-channel effect suppression. On the individual device level, model predictions indicate that the minimum channel length can be scaled beyond 10 nm for a turn-off behavior of S=100 mV/dec for a silicon film thickness below 5 nm and an electrical equivalent oxide thickness below 1 nm. For the purpose of gigascale integration, however, the ability to tightly control process tolerances will determine the ultimate scaling limits on double-gate MOSFETs. The minimum channel length is increased to ~16 nm if a 70 mV voltage variation is allowed for 30% cumulative process tolerance that accounts for both channel length variation and silicon film



8. Scaling limits: (a) channel length versus oxide thickness and (b) channel length versus silicon film thickness.

thickness variation. If novel technologies, such as proposed in [23], are developed to tighten process controls, the feasibility of gigascale integration using undoped DG MOSFETs with a 10 nm channel length can be realized.

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Appendix: Summary of Parameters

For the subthreshold swing model (3):

$$\Gamma_1 = \frac{2\lambda_1}{t_{Si}}\sqrt{1+\frac{t_{Si}^2}{r^2\lambda_1^2}} \Bigg/ \left(\frac{1}{r}+\frac{1}{2}+\frac{1}{2}\frac{t_{Si}^2}{r^2\lambda_1^2}\right).$$

For the threshold voltage model (5):

$$\eta = 1+\frac{2\theta}{r}\tanh\theta,$$

$$\theta = Bt_{Si} / L,$$

$$B = \pi\left(1+2e^{-qV_{bi,i}/2kT}\lambda_{Di} / L\right)^{-1},$$

where $V_{bi,i}$ is the source/drain junction built-in voltage with intrinsic silicon, and λ_{Di} is the intrinsic Debye length given as

$$\lambda_{Di} = \sqrt{2kT\varepsilon_{Si} / q^2 n_i},$$

$$\varphi_{0m} = V_{bi,i} - \frac{2kT}{q}\ln\frac{2+e^{qV_{bi,i}/2kT}L / \lambda_{Di}}{\pi}.$$

Qiang Chen and *James D. Meindl* are with the Microelectronics Research Center, Georgia Institute of Technology, in Atlanta, Georgia, USA. *Keith A. Bowman* was previously with the Georgia Institute of Technology and is now with Intel Corp. in Hillsboro, Oregon, USA. *Evans M. Harrel* is with the School of Mathematics, Georgia Institute of Technology. E-mail: qiang.chen@ece.gatech.edu.

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