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Impact of High-κ Dielectrics on Undoped Double-Gate MOSFET Scaling

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I. Introduction[*]

As conventional bulk MOSFETs scale into the sub-100nm regime, introduction of high-κ gate dielectrics to replace SiO_2 seems imminent to alleviate the ever increasing gate tunneling current [1]. While a thin gate-oxide layer is extremely important to short-channel-effect (SCE) control in bulk devices, it is much less critical in undoped double-gate (DG) MOSFETs [2]. In addition, gate tunneling current in symmetric DG MOSFETs may be smaller than in bulk devices [3]. On the other hand, use of high-κ dielectrics leads to much deteriorated SCEs in DG MOSFETs [4,5]. This paper analyzes in a concerted manner both SCEs and gate tunneling in undoped symmetric DG MOSFETs with candidate high-κ dielectrics that currently receive close attention. To this end, an analytical threshold rolloff (ΔV_{TH}) model with high-κ dielectrics is proposed in Section II that gives close agreement to published numerical simulations. Section III estimates the minimum thickness of the dielectrics under study limited by gate direct tunneling current. Section IV comprehensively assesses the impact of high-κ dielectrics on scalability of DG MOSFETs. Concluding remarks are provided in Section V.

II. High-κ Threshold Rolloff Model

Analytical short-channel threshold (V_{TH}) and rolloff models have been recently developed for symmetric undoped DG MOSFETs with a *thin* gate dielectric layer by solving a 2-D Poisson equation with the mobile charge term included in the channel region [6],

$$\Delta V_{TH}=\left[\frac{kT}{q}\ln\frac{Q_{TH}}{n_i t_{Si}}-\varphi_{0m}\right]\left[\eta\frac{\cosh\theta}{\cosh(\theta/2)}-1\right]\cdot \tag{1}$$

Detailed parameter descriptions are provided in Table 1. Particularly, φ_{0m} is the minimum channel potential. With use of a high-κ dielectric, its increased physical thickness leads to strong two dimensionality of the electric field in the gate dielectric. The resulting fringe field lowers the channel potential barrier (FIBL) [7], thus causing extra SCEs. The FIBL effect can be modeled by increasing the channel potential φ_{0m},

$$\varphi_{0m}\rightarrow\varphi_{0m}+\varsigma(kT/q), \tag{2}$$

where the parameter ζ is heuristically derived as,

$$\varsigma=2.39(t_I/t_{Si})\ln(\varepsilon_I/\varepsilon_{SiO_2})\cdot \tag{3}$$

The resulting high-κ rolloff model is obtained as,

$$\Delta V_{TH}=\left[\frac{kT}{q}\ln\frac{Q_{TH}}{n_i t_{Si}}-\varphi_{0m}-\left(2.39\frac{t_I}{t_{Si}}\ln\frac{\varepsilon_I}{\varepsilon_{SiO_2}}\right)\frac{kT}{q}\right]\left[\eta\frac{\cosh\theta}{\cosh(\theta/2)}-1\right], \tag{4}$$

which gives close agreement with published FIELDAY numerical simulations [4], as demonstrated in Figure 1.

III. Gate Direct Tunneling Current

An analytical model of gate direct tunneling current has been developed in [8],

$$J_T=\frac{4\pi m^* q}{h^3}(kT)^2\left(1+\frac{\gamma kT}{2\sqrt{E_B}}\right)\exp\left(\frac{q\varphi_S-E_g/2}{kT}-\gamma\sqrt{E_B}\right)\cdot \tag{5}$$

Parameter descriptions are provided in Table 1. The surface potential φ_S is obtained by solving a 1-D Poisson equation with the mobile charge term only in the channel under the *strong* inversion condition [9]. Applying (5), the gate tunneling current versus equivalent oxide thickness (EOT, $t_{ox,eq}$) is calculated for SiO_2 and three candidate high-κ dielectrics (Figure 2), $HfSiO_4$, Al_2O_3, and HfO_2, whose material parameters are summarized in Table 2 [10,11]. The minimum EOT for each dielectric is estimated at J_T=1A/cm^2 [12] and marked in Figure 2.

IV. High-κ Impact on Scalability

The total impact of high-κ dielectrics on undoped DG MOSFETs can be assessed by evaluating the minimum channel length (L) constrained by both FIBL-enhanced SCEs and gate tunneling current. For this purpose, the minimum channel length is determined as such that V_{TH} variation reaches 70 mV when the channel-length-equivalent parameter variation is 30% [6]. Applying (4), L versus EOT characteristics are obtained with t_{Si}=10nm for all four gate dielectrics, as shown in Figure 3a. At the same EOT, high-κ dielectrics significantly increase the minimum channel length. A much smaller EOT of a high-κ dielectric than that of SiO_2 is therefore required for a given channel length. Although a larger gate capacitance consequently results, it may not lead to significant improvement in the drive current unless the channel mobility degradation can be resolved [1]. At their own smallest EOTs allowed by gate tunneling current (marked by discrete points in Figure 3), high-κ dielectrics reduce the minimum channel length from 39nm as of SiO_2 by 3.6nm, 6.7nm, and 6.4nm or 9%, 17%, and 16% for $HfSiO_4$, Al_2O_3, and HfO_2, respectively. While such channel length

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reductions provide noticeable improvement, they fall well short of the 30% that MOSFET scaling used to achieve between technology nodes. A similar study carried out for t_{Si}=3nm, which is at the ultimate scaling limit for DG MOSFETs, leads to the same observations (Figure 3b) with $HfSiO_4$, Al_2O_3, and HfO_2 providing 3%, 18%, and 12% channel length reduction, respectively.

V. Summary/Conclusions

An analytical threshold rolloff model for symmetric undoped DG MOSFETs with high-κ dielectrics has been derived that gives close agreement with published numerical simulations. A concerted analysis of both FIBL-enhanced SCEs and gate tunneling current involving representative high-κ dielectrics ($HfSiO_4$, Al_2O_3, and HfO_2) shows that their substitution for SiO_2 helps scale the minimum channel length, but only by less than 20%. Additional drive current improvement from reduced EOTs is contingent upon resolution of channel mobility degradation caused by high-κ dielectrics.

References

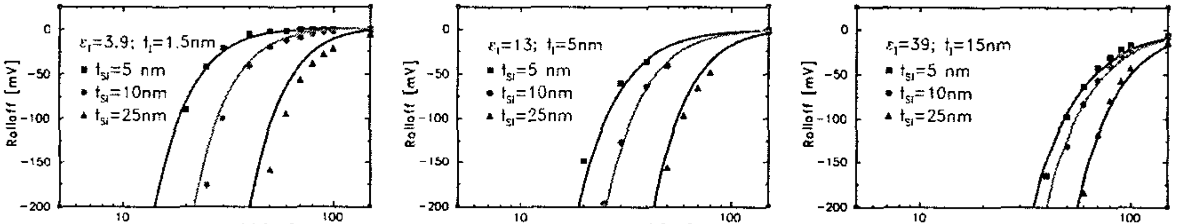
[1] E. P. Gusev et al., *IEDM*, 2001, pp. 451-454.
[2] Q. Chen et al., *Proc. Int. SOI Conf.*, 2002.
[3] L. Chang et al., *IEDM*, 2001, pp.99-102.
[4] D. J. Frank et al., *IEEE EDL*, vol. 19, no. 10, pp. 385-387, Oct. 1998.
[5] H.-S. P. Wong et al., *IEDM*, 1998, pp. 407-410.
[6] Q. Chen et al., sub. *IEEE T-ED*, 2002.
[7] G. C.-F. Yeap et al., *Elec. Letters*, vol. 34, no. 11, pp. 1150-1152, May 1998.
[8] K. A. Bowman et al., *IEEE T-ED*, vol. 48, no. 8, pp. 1800-1810, Aug. 2001.
[9] Y. Taur, *IEEE EDL*, vol. 21, no. 5, pp. 245-247, May 2000.
[10] C. M. Osburn et al., *IBM J. Res. & Dev.*, vol. 46, no. 2/3, pp. 299-315, Mar./May 2002.
[11] Y. Harada et al., *Symp. VLSI Tech. Dig. Tech. Papers*, June 2002, pp. 26-27.
[12] Y. Taur et al., *Proc. IEEE*, vol. 85, no. 4, pp. 486-504, April 1997.

Table 1. Summary of model parameters.

Rolloff model: n_i is intrinsic density of electrons; q is electron charge; k is Boltzmann constant; T is temperature; Q_{TH} is a constant inversion charge sheet density; ε_I and t_I are permittivity and thickness of gate dielectric; ε_{Si} and t_{Si} are permittivity and thickness of Si; L is channel length; $V_{bi,i}$ is junction built-in voltage with intrinsic Si; λ_{Di} is intrinsic Debye length.

$$\eta = 1+\frac{2\theta}{r}\tanh\theta;\quad r=\frac{\varepsilon_I t_{Si}}{t_I\varepsilon_{Si}};\quad \theta=\frac{Bt_{Si}}{L};\quad B=\pi\left(1+2e^{-qV_{bi,i}/2kT}\lambda_{Di}/L\right)^{-1};\quad \lambda_{Di}=\sqrt{2kT\varepsilon_{Si}/q^2n_i};\quad \varphi_{0m}=V_{bi,i}-\frac{2kT}{q}\ln\frac{2+e^{qV_{bi,i}/2kT}L/\lambda_{Di}}{\pi}.$$

Gate tunneling model: h is Planck constant, m^* is electron transverse mass in Si, φ_S is surface potential, χ is conduction band offset of dielectric with respect to Si, E_g is Si band gap, V_{gs} is gate voltage, E_B is average rectangular barrier height, m_I is effective electron mass in dielectric, $\Phi_{MS,i}$ is gate work function referenced to intrinsic Si. $E_B=\chi-q(V_{gs}-\Phi_{MS,i}-\varphi_S)/2$; $\gamma=4\pi t_I(2m_I)^{1/2}/h$.



(a) (b) (c)

Figure 1. Threshold rolloff with different dielectric permittivity values. Solid lines are the analytical model (4). Discrete points in (a) and (c) are published FIELDAY numerical simulations [4]; discrete points in (b) are Medici simulations.

Table 2. Gate dielectric parameter summary

Material	SiO_2	$HfSiO_4$	Al_2O_3	HfO_2
Permittivity (ε_I) [10]	3.9	12 [11]	12	22 [11]
Conduction band offset (χ), eV [10]	3.15	1.5	2.8	1.5

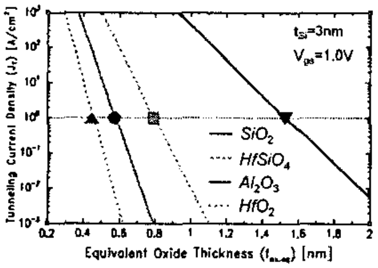
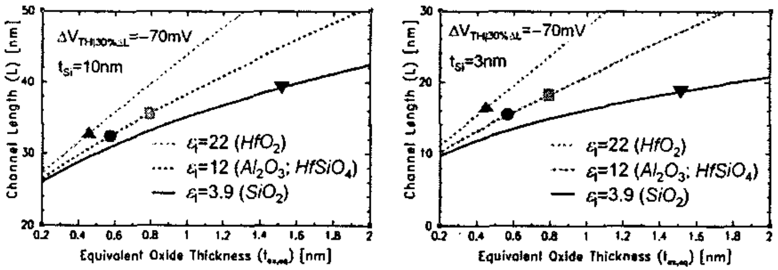


Figure 2. Gate tunneling current density versus EOT. Symbols: min. EOTs.



(a) (b)

Figure 3. Channel length versus EOT: (a) t_{Si}=10nm; (b) t_{Si}=3nm. Symbols mark data points with minimum EOTs: ▼- SiO_2; ■ – $HfSiO_4$; ● - Al_2O_3; ▲ - HfO_2.