

'Trimodal' Wafer-Level Package: Fully Compatible Electrical, Optical, and Fluidic Chip I/O Interconnects

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Abstract:

We describe the fabrication, assembly, and testing of a wafer-level package with fully compatible electrical, optical, and fluidic ('trimodal') chip I/O interconnects. Various trimodal interconnect configurations are introduced. The trimodal I/Os are fabricated using five minimally demanding masking steps. In order to experimentally characterize the trimodal I/Os, we fabricate two separate substrates to test the chips with these I/Os in a piecewise manner. In the first assembly demonstration, we perform electrical and optical I/O interconnection measurements. In the second assembly demonstration, we perform electrical and fluidic interconnection measurements. Measurements reveal that the metal-clad optical pins (55x110 μm in size) attenuate an optical signal (632.8 nm wavelength) by 3.6 %. The electrical resistance is measured to be 50 m Ω . It is also shown that the fluidic I/Os with the integrated back-side thermofluidic microchannel heat sink can achieve thermal resistance as low as 0.17 $^{\circ}\text{C}\text{-cm}^2/\text{W}$. Cooling of localized power density of $>300 \text{ W/cm}^2$ is also demonstrated. Mechanical testing of polymer pins before and after metallization is also reported.

I. Introduction

The performance and cost of silicon ancillary technologies have not scaled in the same way that silicon technology has. Historically, shrinking of the minimum feature sizes of a transistor have led to increased switching speed, lowered energy dissipation per switching operation, and decreased cost per transistor. These results are the basis of Moore's Law, which asserts that the transistor density in a chip doubles every 18 months. Remarkably, Moore's Law has accurately projected the integration trend of integrated circuits (ICs) for more than 40 years. Today, billion-plus transistor multiprocessors are available on the market.

However, while silicon technology has continued to progress at a very rapid pace, silicon ancillary technologies have scaled in reverse. The inability to remove heat, provide high-bandwidth off-chip interconnects, and efficiently deliver power to a gigascale system have imposed significant constraints on system performance. According to the International Technology Roadmap for Semiconductors (ITRS) [1], the projected junction-to-ambient thermal resistance will be less than 0.2 $^{\circ}\text{C}/\text{W}$ by the end of the roadmap. Moreover, it is projected that high-performance chips will drain more than 280 A at 0.7 V. With respect to signaling, it is projected that off-chip communication frequency will be greater than 80 GHz (for a small number of I/Os). Meeting the heat removal, power delivery, and off-chip signaling requirements simultaneously motivates the need to explore disruptive new silicon ancillary technologies.

In this paper, we describe low-cost fully compatible electrical, optical, and fluidic (trimodal) chip I/O interconnects to address the power delivery, off-chip bandwidth, and cooling requirements, respectively, of gigascale systems at the end of the roadmap. This paper is organized as follows: Section II presents various trimodal I/O interconnect configurations. Fabrication details of the trimodal I/Os and the package substrate are described in Section III. Optical and thermal measurements are reported in Sections IV and V, respectively. Mechanical compliance measurements of metal-coated polymer pins are reported in Section VI. Finally, Section VII is the conclusion.

II. Trimodal I/O Interconnect Configurations

In this section, we describe various trimodal I/O interconnect configurations. Figure 1 is a schematic illustration of a silicon die with trimodal I/O interconnects. The building block of this approach is based on the fabrication of high aspect-ratio polymer pins. The intrinsic function of a polymer pin is to provide a mechanically flexible surface-normal optical waveguide between the chip and the package substrate [2, 3]. We have previously demonstrated that the polymer pins enhance the coupling efficiency between a light source and an optical aperture (to emulate a photodetector) by up to 4.5 dB compared to direct free-space coupling [4]. Moreover, due to the flexible nature of the polymer pins, it was also demonstrated that the optical polymer pins can maintain high coupling efficiency between the chip and substrate during misalignment, which may be induced due to the coefficient of thermal expansion (CTE) mismatch between the die and package substrate. It was shown that for a 30 μm misalignment, a 50x150 μm polymer pin maintains optical interconnection and incurs only a 1 dB loss [4, 5].

Using the polymer pin as the building block, electrical I/O interconnects are achieved by depositing metal on the polymer pins. The microfluidic I/Os are achieved through the fabrication of hollow-core polymer pins, or micropipes [6, 7]. A critical feature of the fluidic I/Os is the back-side silicon-based and integrated heat sink to which they interface using through-silicon vias [8]. No thermal-interface material (TIM), which can limit performance and reliability [9], is used as the microchannel heat sink is fabricated directly in the silicon die using wafer-level batch fabrication. Using the fluidic I/Os, a coolant can be channeled from substrate-level fluidic interconnects to the microchannel heat sink in an efficient and reliable way. The monolithic fabrication of a microchannel heat sink in an IC was first demonstrated in [10] and has inspired much recent research in microchannel heat sinks based on their work [11-16]. However, the topics of fluidic I/Os and how to deliver the fluid in and out of the chip in a

way that is compatible with CMOS technology and conventional off-chip interconnects have not been discussed. In the proposed fluidic I/O configuration, no bulky external fluidic tubes are needed, as is common in previous research.

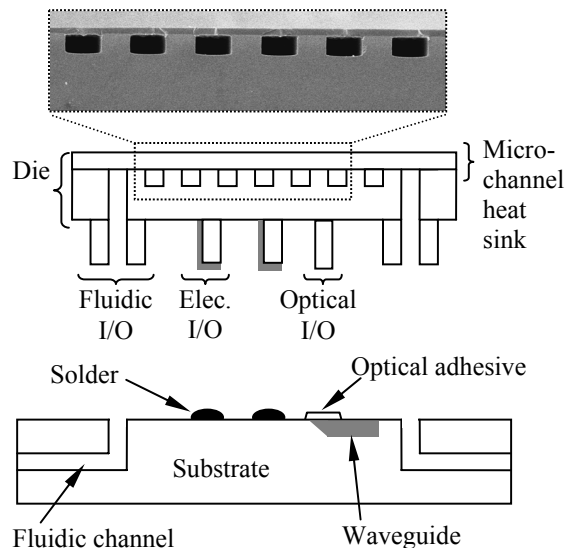


Figure 1: Schematic illustration of a silicon die with fully compatible electrical, optical, and fluidic I/O interconnects. The basic building block of the I/Os is the fabrication of a high-aspect ratio polymer pin.

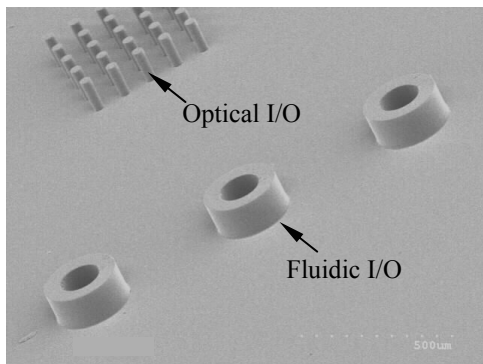


Figure 2: SEM image of relatively low-aspect ratio (3:1) surface-normal optical waveguides adjacent to microfluidic I/O interconnects. The I/Os were fabricated using the polymer Avatrel. The optical pins are 35 μm in diameter and 110 μm in height, and the fluidic I/Os have an inner diameter of 150 μm and are 110 μm in height.

The fabrication of the trimodal I/Os utilizes wafer-scale batch processing and will be described later in the paper. SEM images of optical and fluidic I/Os are shown in Figure 2 and Figure 3. The I/O interconnects shown in Figure 2 were fabricated using the polymer Avatrel [17]. Because it is a low-modulus polymer, the aspect ratio of the I/Os is limited by the strength of the I/Os to hold their own weight before buckling. As a result, the I/Os are relatively low-aspect ratio (3:1). The I/O interconnects shown in Figure 3 were fabricated using SU-8 [18], which has a modulus that is 8-times larger (4 GPa) than that of Avatrel (0.5 GPa). Thus, it was possible to

fabricate very high-aspect ratio I/O interconnects (7:1 shown in Figure 3).

Another approach for integrated trimodal I/Os is shown in Figure 4. In this approach, polymer pins are each used to provide two (dual) interconnect functions between the chip and package substrate. Sidewall metallized optical and fluidic pins are used to provide electrical-optical [19] and electrical-fluidic interconnections, respectively. SEM images of such I/O interconnects are shown in Figure 5 and Figure 6.

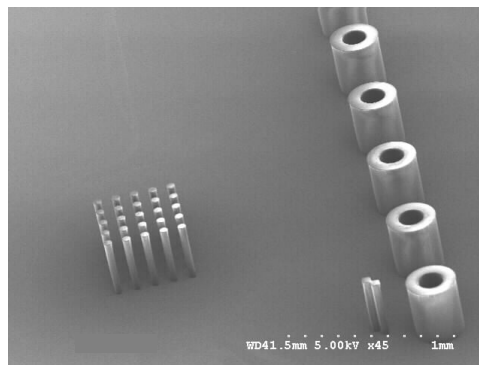


Figure 3: SEM image of relatively high-aspect ratio (7:1) surface-normal optical waveguides adjacent to microfluidic I/O interconnects (using same photomask used to fabricate the I/Os shown in Figure 2). The I/Os were fabricated using SU-8.

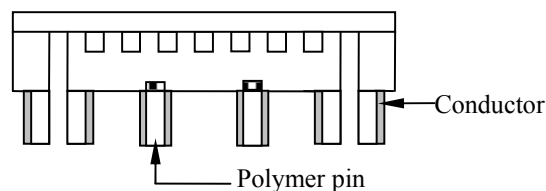


Figure 4: Schematic illustration of a silicon die with fully compatible electrical, optical, and fluidic I/O interconnects using dual-modal I/Os. The electrical interconnects are constructed by depositing metal on the sidewalls of the polymer pins.

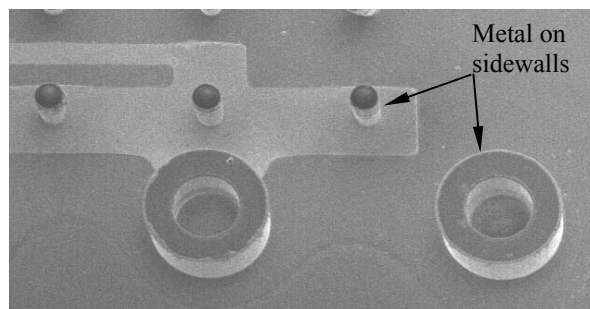


Figure 5: SEM image of sidewall metallized optical and fluidic chip I/O interconnects. This approach enables both the optical and fluidic I/Os to simultaneously transmit an electrical signal. As such, each I/O provides more than a single interconnection and thus, are called dual-mode I/Os.

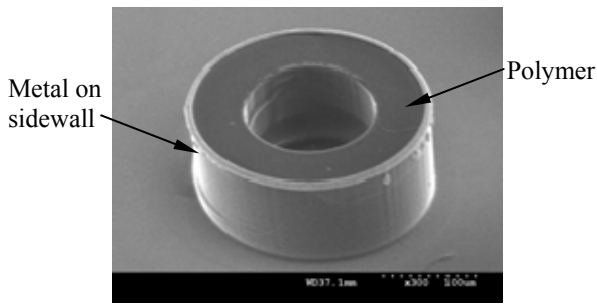


Figure 6: High-magnification SEM image of the sidewall-metallized micropipes shown in Figure 5.

III. Fabrication of Trimodal Chip I/O Interconnects and Substrate-Level Interconnects

The process used to fabricate the trimodal I/Os shown in Figure 4 is illustrated in Figure 7. The fabrication process of the trimodal I/Os is implemented following the end of semiconductor back-end-of-the-line (BEOL) processing. It is assumed that optical devices (sources and/or detectors) are either monolithically or heterogeneously integrated on the silicon chip. The first process step (Figure 7b) is to fabricate the back-side microchannel heat sink and through-wafer fluidic vias and the details of which were previously described [6, 8]. Next, a polymer film is spin coated on the front-side of the chip and patterned into the optical and fluidic polymer pins (Figure 7c). The pins have been fabricated using both Avatrel and SU-8, both of which are photodefinable. Next, using photolithography, a metal film is deposited on the polymer pins and patterned such that the metal is etched from the tip but remains on the sidewalls of the polymer pins (Figure 7d).

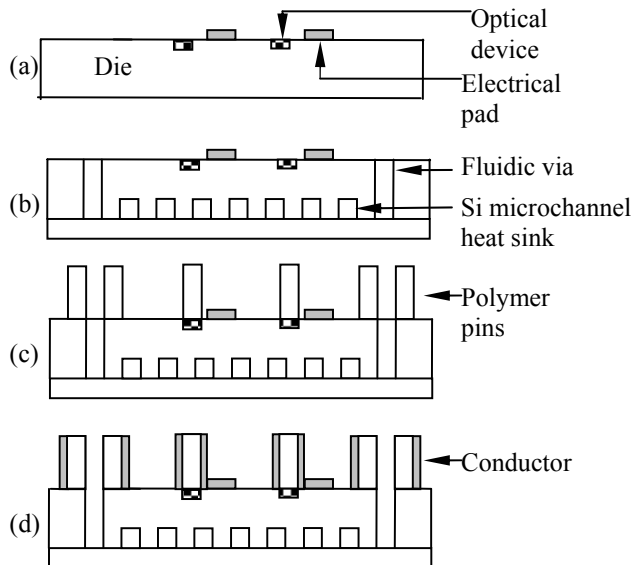


Figure 7: Schematic illustration of the fabrication process used to fabricate the trimodal I/Os based on the configuration shown in Figure 4.

It is clear that in order to assemble such a die it is critical to have a package substrate with trimodal planar interconnects. While substrate-level optical waveguides have

been widely studied [20-24], integrated electrical, optical, and fluidic interconnects are not reported, particularly for IC packaging. The previously reported air-gap technology for optical waveguides [20] provides an opportunity to simultaneously fabricate optical and fluidic interconnects. In this work, the same sacrificial polymer is patterned to create air-gaps on a substrate for the polymer waveguides (cladding) as well as to form fluidic channels, as shown in Figure 8. Figure 9 is an optical micrograph of the substrate at step (d) in the fabrication process flow shown in Figure 8. Figure 10 illustrates cross-sectional SEM micrographs of the air-gaps for the optical and fluidic interconnects.

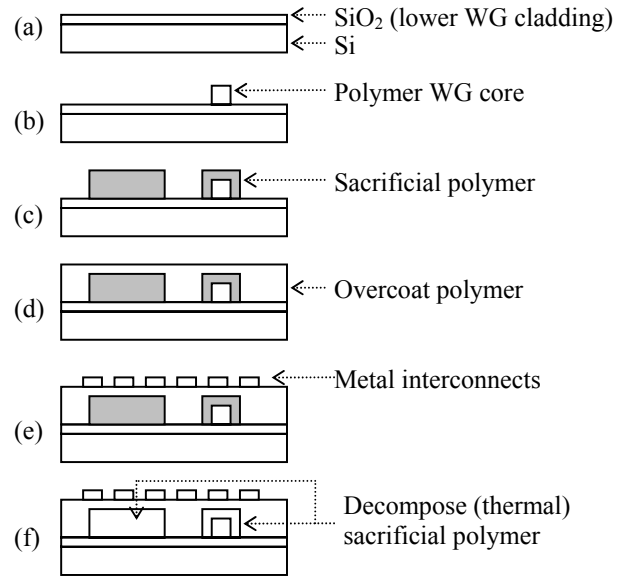


Figure 8: Schematic illustration of the process used to fabricate a package substrate with electrical, optical, and fluidic microscale interconnects. {WG: waveguide}

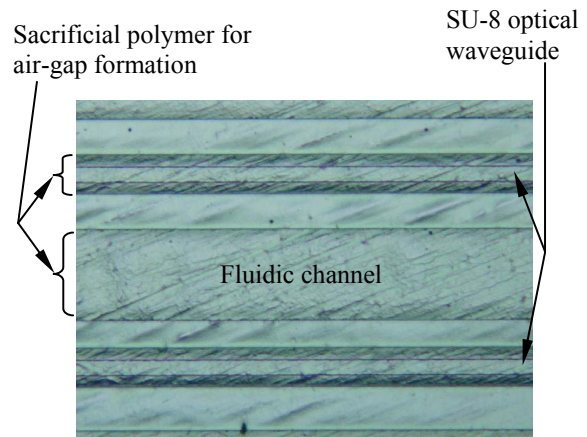


Figure 9: Optical micrograph of a package substrate at step (d) of the fabrication process show in Figure 8.

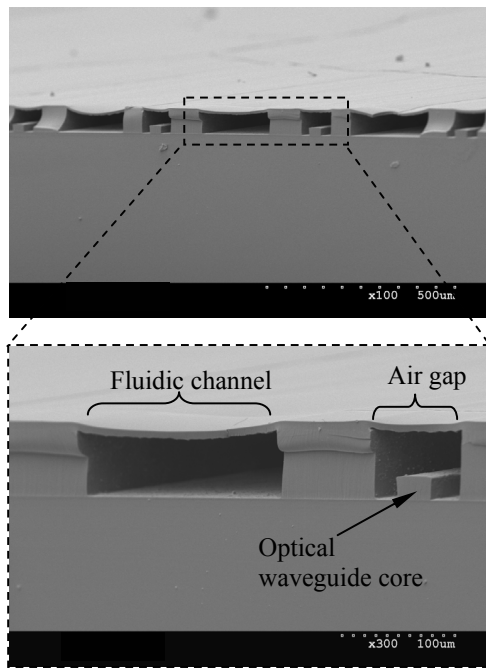


Figure 10: Cross-sectional SEM micrographs of the air-gaps that are fabricated simultaneously to enable air-clad optical waveguides and microfluidic channels. Electrical interconnects are not shown.

IV. Optical Coupling Measurements

In an effort to test the trimodal I/Os in a piecewise manner, the first set of measurements deals with the electrical and optical interconnects. The optical power transmission loss through the dual-mode polymer pins was measured first. For this measurement, the polymer pins were fabricated above metal apertures on a transparent glass substrate to permit optical access to both ends (Figure 11). The test sample was fabricated by first depositing and patterning a metal film on a glass substrate. In this case, a 30 nm/400 nm/30 nm Ti/Au/Ti metal film stack was used. Next, silicon dioxide is deposited above the patterned metal film to enhance the adhesion of the polymer pins to the substrate. The fabrication steps described in the previous section are next used to fabricate the dual-mode polymer pins (110 μm tall and 55 μm in diameter). Following the fabrication, a single-mode fiber (632.8 nm wavelength) was used to measure optical loss through the dual-mode polymer pin (which also includes the glass substrate) and the open metal aperture. The measurement approach was to first place the optical fiber directly above the aperture and measure the maximum intensity transmitted through it using the detector. This was repeated for multiple apertures and an average was taken. Next, the fiber was placed directly above the pins and the intensity maximized and measured. Again, this was repeated for multiple pins and an average was taken. The average pin-transmitted intensity for five pins was measured with respect to the average aperture-transmitted intensity for five apertures. In this way, the average measured optical intensity reduction from the set of five measurements is 3.6%. Given that the optical polymer pin can enhance coupling efficiency by more than 4 dB [4], the 3.6% loss is minimal compared to its benefits.

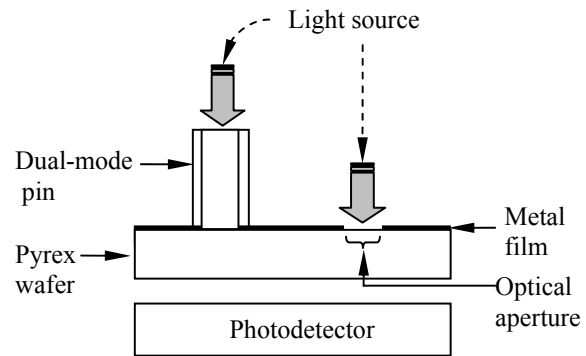


Figure 11: Experimental setup used to measure optical power losses through the metal-clad polymer pins.

For successful assembly and testing of the dual-mode pins, mirror terminated waveguides were fabricated on a silicon substrate, as illustrated in Figure 12. The process that was used to integrate mirrors with the waveguides is shown in Figure 13 and is an extension of previous work [25]. The waveguide core was photopatterned using SU-8 and was 20 μm thick and 40 μm wide. The waveguide cladding (Avatrel) was spin coated above the SU-8 waveguide core to a 25 μm thickness. Vias were next photopatterned through the cladding layer directly above the mirrors. To provide simultaneous electrical and optical interconnection through each dual-mode pin, Cu pads (1 μm thick), each with a via equal in diameter to that of the polymer pins, were fabricated above the via in the cladding layer (Figure 12 and Figure 13). A 15 μm thick layer of solder (60/40 Sn/Pb) was electroplated on the Cu pads. The resulting solder resembled a ring-pattern, as illustrated in Figure 14. The die and substrate shown in Figure 12 were assembled using a flip-chip bonder. The bonding profile (temperature and force) was selected to control the substrate-level solder during reflow: the chip and substrate were brought into contact before elevating the temperature to the solder melting temperature (180°C). Under compression (150 g), the chip and substrate were heated to the reflow temperature (220°C), which is well below the glass transition temperature (250°C) of the polymer used for the fabrication of the polymer pins. Not only does the solder provide an electrical path between the pins and the electrical wiring on the substrate, but also mechanically attaches the optical I/Os to the waveguide. Using the electrical interconnects on the substrate, the measured electrical resistance of the dual-mode pins is 50 m Ω . To demonstrate simultaneous optical coupling, a single mode optical fiber was used to excite the planar waveguide. Power from the resulting waveguide mode was then reflected by the mirror into the dual-mode polymer pin. A CCD digital camera was used to capture the resulting transmitted light, as shown in Figure 15, to qualitatively demonstrate functionality. This was demonstrated by illuminating four adjacent waveguides and light was observed outcoupled from each corresponding pin through the glass chip, as shown in Figure 15. Quantitative power measurements are a next step in this work. However, optical simulations demonstrate that the coupling efficiency between a waveguide and a polymer pin can be as high as 89% when using the mirrors described in [25].

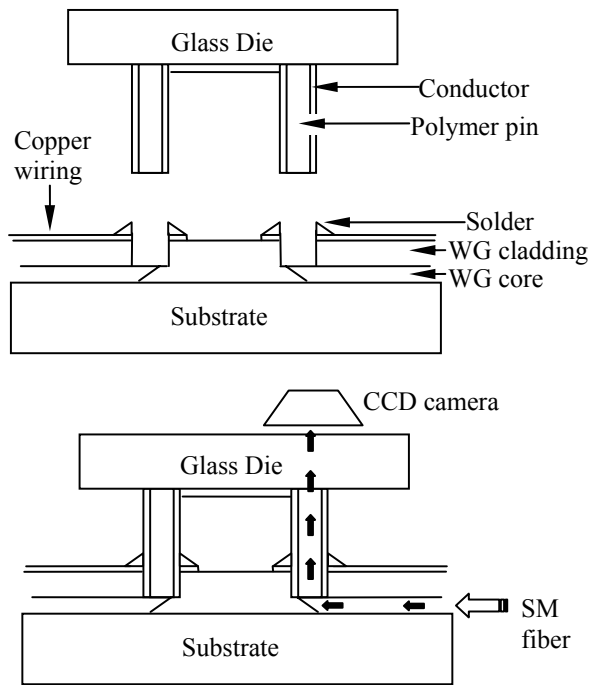


Figure 12: Schematic of the experimental setup used to measure electrical continuity through a pair of dual-mode I/Os and demonstrate optical coupling from a planar waveguide and the dual-mode I/O. {WG: waveguide; SMF: single-mode fiber }

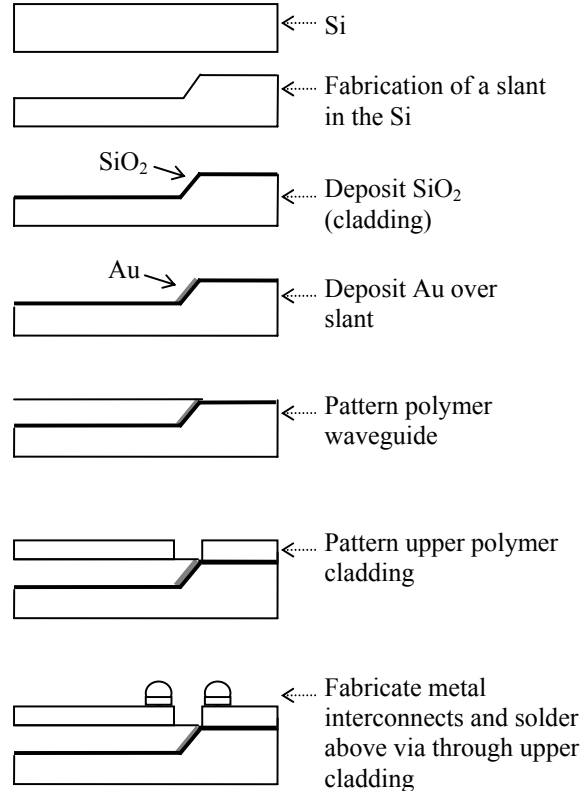
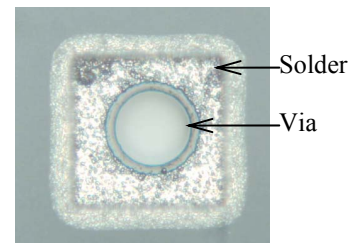
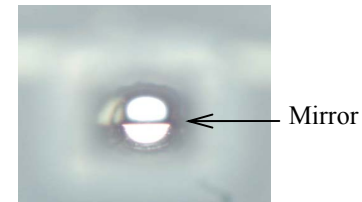


Figure 13: Schematic illustration of the process used to fabricate mirror terminated waveguides to receive the dual-mode electrical-optical chip I/O interconnects.



Focused on pad at top of via



Focused on mirror at base of via

Figure 14: Optical images of annular shaped metallic (solder) pads fabricated around a via through the cladding layer of the waveguide.

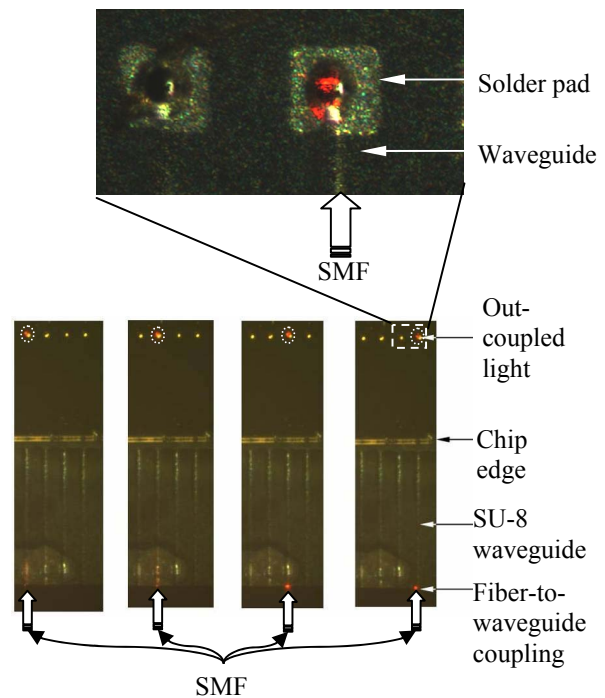


Figure 15: CCD image of the transmitted light through the dual-mode polymer pin. {SMF: single-mode fiber }

V. Thermal Measurements

Once again, in an effort to test the trimodal I/Os in a piecewise manner, the second set of measurements deals with the electrical and fluidic interconnects. In order to experimentally characterize the thermofluidic interconnect networks, thin-film Pt heaters/thermometers were fabricated on the chip. The experimental setup is shown in Figure 16. Solder bumps were used for the electrical I/Os. There are a total of 51 parallel microchannels (100 μm in width and 200 μm in height) distributed evenly across the back-side of the

chip (1 cm^2), and a total of 32 fluidic I/Os were used. It is important to note that the heat sink has not been optimized for lowest thermal resistance and pressure drop. The inlet and outlet temperatures were measured using thermocouples. The chip temperature was measured manually by recording the change in the resistance of the heaters.

The on-chip temperature as well as the outlet temperature increased rapidly once power was applied to the heaters. Under a larger flow rate ($\sim 104 \text{ ml/min}$), the average temperature rise is $12.7 \text{ }^\circ\text{C}$ and the corresponding thermal resistance for the chip is $0.28 \text{ }^\circ\text{C/W}$, which translates to a unit thermal resistance as small as $0.17 \text{ }^\circ\text{C-cm}^2/\text{W}$. An important benefit of using an on-chip microchannel heat sink is to enable the cooling of highly localized power density (or hot spots). Figure 17 shows the measured temperature rise of a small area ($\sim 0.08 \text{ cm}^2$) as a function of power density. As expected, the measured temperature rise on the heaters increases with increasing localized power density, and the temperature rise is reduced as the DI water flow rate increases. Under a larger flow rate, the ΔT -pressure curve becomes nearly linear and a localized power density larger than 325 W/cm^2 was tested with a temperature rise of $46 \text{ }^\circ\text{C}$ at a flow rate of 125 ml/min . These results clearly demonstrate the feasibility of the proposed fluidic I/O interconnects, their compatibility with flip-chip technology, and functionality.

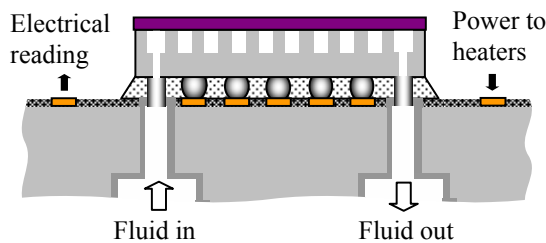


Figure 16: Schematic illustration of the experimental setup used to measure the temperature vs. power data.

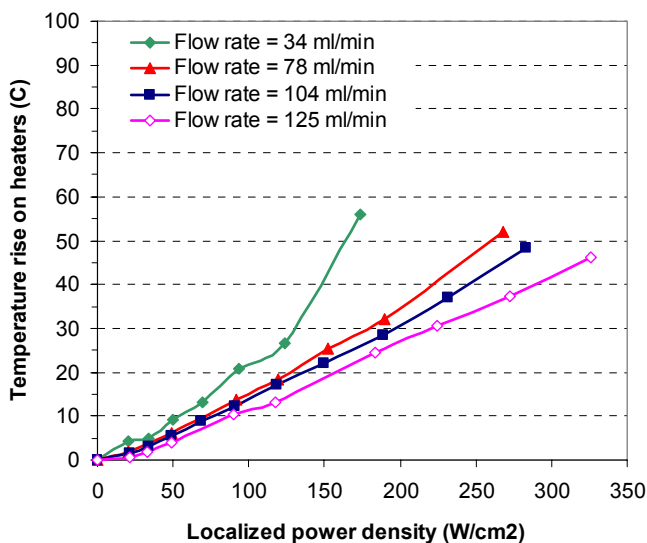


Figure 17: On-chip temperature rise as a function of localized heating power under various DI water flow rates (with localized heating area of $\sim 0.08 \text{ cm}^2$).

VI. Lateral Mechanical Compliance Measurements of Metal-Coated Polymer Pins

In order to measure the lateral force-displacement characteristic curve of polymer pins with and without metal coating, a silicon die containing the I/Os was mounted sideways in a Hysitron TriboIndenter, as shown in Figure 18. The peak displacement of the I/Os was limited by the test equipment and is equal to $5 \text{ }\mu\text{m}$, in this case. Polymer pins with (Ti/Au, $500 \text{ \AA}/0.8 \text{ }\mu\text{m}$) and without metal were tested using this experimental setup. Figure 18 illustrates a micrograph of the sideways-mounted metal-coated polymer pin in the TriboIndenter. Results for both interconnects are shown in Figure 19. The data (Figure 19) for the metal-free polymer pin (intrinsic, air-clad) undergoes elastic deformation up to the $5 \text{ }\mu\text{m}$ peak displacement possible with the test equipment. As indicated by the unload curve, the polymer pin returns to its original position following the removal of the load. The compliance of the interconnect can be calculated by dividing the maximum elastic displacement at the peak measured force and is equal to $2.17 \text{ }\mu\text{m/mN}$. The compliance of the pins significantly increases as their length (height) increases or as their diameter decreases [2, 26]. The force-displacement characteristic curve of the metal-coated polymer pin is also shown in Figure 19 for comparison. The force required to attain the same displacement has increased by approximately a factor of two. Moreover, the unload curve of the metal-coated polymer pin illustrates plastic deformation, which is visible by the slope of the unload curve. As a result, these measurements illustrate the trade-offs between the electrical and mechanical characteristics of the dual-mode I/Os. Optimization of all I/O interconnects will be reported in the future.

VII. Conclusion

We describe the fabrication, assembly, and testing of a novel wafer-level package technology that provides fully compatible and low cost electrical, optical, and fluidic, or ‘trimodal,’ chip I/O interconnects. The building block of the trimodal I/Os approach discussed in this paper is high-aspect ratio polymer pins. We demonstrated the assembly of the trimodal I/Os in a piecewise manner. First, electrical and optical interconnections were demonstrated. This required the fabrication of a substrate with compatible electrical and optical interconnects. The measured electrical resistance of the dual-mode I/Os was $50 \text{ m}\Omega$. Optical interconnection between the substrate-level waveguides and the assembled dual-mode I/Os was qualitatively demonstrated. The optical transmission losses through the dual-mode I/Os were shown to be less than 3.6%. In the second demonstration, electrical and fluidic interconnections were demonstrated. Thin-film Pt thermometers and heaters were integrated on-die to enable temperature vs. power measurements and characterize the performance and compatibility of the proposed fluidic interconnects. It was shown that under a larger flow rate ($\sim 104 \text{ ml/min}$), the average temperature rise is $12.7 \text{ }^\circ\text{C}$ and the corresponding thermal resistance for the chip is $0.28 \text{ }^\circ\text{C/W}$, which translates to a unit thermal resistance of $0.17 \text{ }^\circ\text{C-cm}^2/\text{W}$. Lower thermal resistance, as previously demonstrated [10], can be achieved with an optimized heat sink design. With these two assembly demonstrations, the proposed

interconnect and packaging technologies represent revolutionary silicon ancillary technologies to simultaneously address the heat removal, power delivery, and high-bandwidth signaling needs of future high-performance chips.

Acknowledgments

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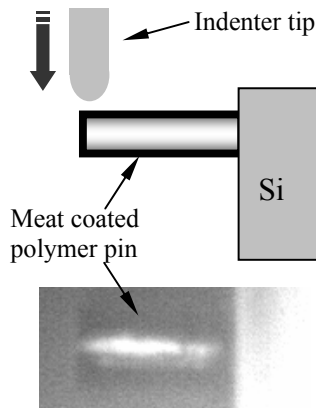


Figure 18: Experimental setup used to test the mechanical compliance of the polymer pins. Also shown is a micrograph of a sideways-mounted 110 μm tall and 55 μm wide metal-coated polymer pin.

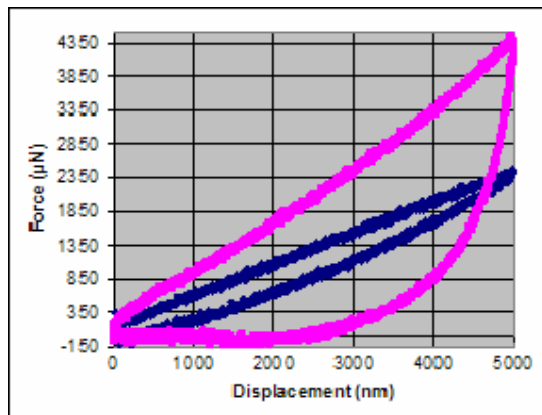


Figure 19: Force-displacement characteristic curve of the sideways mounted and fully metallized polymer pin (top curve). For comparison, the force-displacement characteristic curve of the same height polymer pin is also plotted (center curve). It is clear that the metallized polymer pin undergoes partial plastic deformation.

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