

Polymer Pillars as Optical I/O for Gigascale Chips using Mirror-Terminated Waveguides

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ABSTRACT

Polymer pillars are chip-level optical I/Os that provide spatial confinement of light propagating between a chip and a board/substrate. The integration of polymer pillars and mirror-terminated waveguides is presented. Pillars are fabricated directly above the metallized anisotropically-etched silicon sidewalls that terminate the waveguides. The mirror angle is 54.74° , yet the presence of the pillar produces a 90° bending of the light. Enabled by mirror-terminated waveguides, polymer pillars represent a promising optical I/O technology for GSI.

I. INTRODUCTION

With changing technology generations, the demand for low-loss, high-speed, and high-bandwidth communication is drawing ever closer to GSI chips. This trend is evident in symmetric multiprocessors, which historically have been built by assembling single-core processor chips, memory, and controllers onto a board. However, increased transistor count has led to multiple processors, memory, and controllers on a single die as with the IBM Power5 [1]. This places great bandwidth demands on chip-board electrical interconnects. It has been shown that these interconnects may impose limits on providing increased bandwidth as transmission rates grow due to high-frequency material losses on the board [2], [3]. As the authors of [3] show, a $203 \times 17.8\mu\text{m}$ copper trace that is 40cm long suffers a 20dB loss at 10GHz on FR-4. This is a challenge as the International Technology Roadmap for Semiconductors projects that chip-board speed will be around 56GHz by the 18-nm technology node [4]; hence, it implies that new interconnect technologies are required. The authors of [2] have shown that a partition length exists at the board level for which optical waveguides provide higher bandwidth than equivalently sized electrical wires. As such, optical interconnects may solve this bandwidth problem.

To motivate their use, optical interconnects must be compatible with conventional electrical packaging and assembly schemes. A critical requirement for chip-to-chip optical interconnection is out-of-plane coupling for directing light between the chip and the board. An example includes bonding detector and VCSEL arrays onto a microprocessor that is attached to an interposer, which is bonded to a board with mirror-terminated waveguides [5]. Another example is the attachment of different chips on a single board using compliant interconnects and volume-grating couplers [6]. These are quasi-free-space solutions because light is not confined between the chip and the board. As such, alignment tolerances are tight due to the coefficient of thermal expansion (CTE) mismatch between the chip and the board. A wafer-level package technology called polymer pillars [7], [8], attempts to resolve these issues.

A polymer pillar is a cylindrical structure that is designed to provide optical and electrical I/O interconnection between a chip

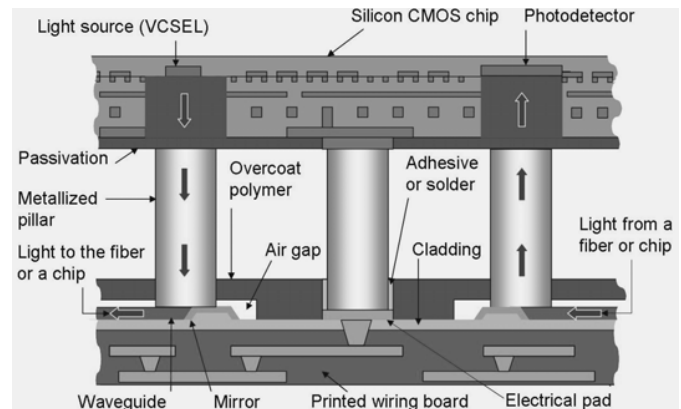


Figure 1. A CMOS chip with monolithically integrated VCSELs and photodetectors attached to a board using dual-mode pillars to provide electrical interconnection and optical interconnection through mirror-terminated waveguides.

and a substrate. Pillars are photolithographically defined at the wafer level in Avatrel 2000P from Promerus LLC., and their densities can exceed $10^5/\text{cm}^2$ [8]. As polymers, their compliant nature accommodates the CTE mismatch between substrates. Optical interconnection is provided because the pillar confines the light along its height due to an index contrast or the presence of metal. Once its sidewalls are metallized, a pillar is also an electrical interconnect because it allows current flow along its periphery. Thus, a single structure provides electrical, optical, and/or both (dual-mode) simultaneously. A GSI chip with dual-mode pillars is depicted in Figure 1, where the chip is assumed to have monolithically integrated detectors [9] and VCSELs [10]. As depicted in the figure, mirror-terminated waveguides on the board are used to couple light into and out of the chip. The waveguides are embedded in air to provide a high index contrast. The waveguide-mirror-pillar coupler configuration is isolated, fabricated, and optically tested herein. The paper is organized as follows: Section II explains how a non- 45° mirror, waveguide, and pillar produce a 90° bending of the light; Section III discusses the fabrication of the coupler configuration; Section IV discusses the optical testing of this configuration; and Section V presents concluding remarks.

II. THE POLYMER PILLAR EFFECT

The optical transmission characteristics of air-clad polymer pillars have been analyzed in [11] to show that they are good waveguides. Hence, the pillar spatially confines light propagating between a chip and a substrate. To enable their use as optical I/O, light is coupled into and out of them using substrate-level mirror-terminated waveguides. From geometric optics we know that a ray incident on a mirror is reflected at an

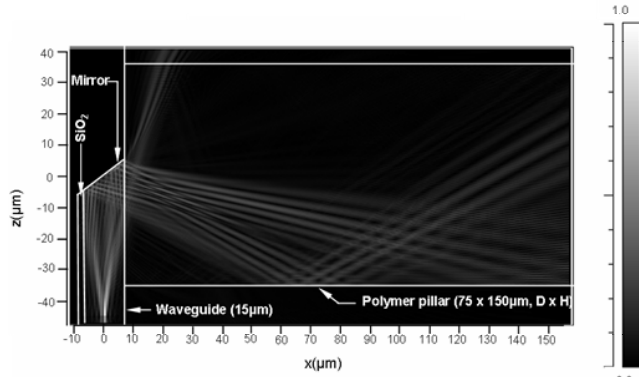


Figure 2. The time-averaged continuous-wave TE simulation result of waveguide-to-pillar coupling using a 54.74° mirror.

angle equal to its incident angle. A 45° angle is therefore the intuitive choice for a mirror aimed at coupling light out of a waveguide at 90° . However, in this work, a metallized anisotropically-etched silicon surface that is at 54.74° with respect to the substrate is used. This mirror is chosen for two reasons: a) as reported in [12], 45° mirror fabrication is difficult and can lead to rough mirror surfaces and b) when the silicon mirror, waveguide, and pillar are integrated, the combination produces a 90° bending of the light – this is because the pillar confines the light entering it due to the mirror. Figure 2 illustrates this last point. It shows a 2D finite difference time domain transverse electric (TE) time-averaged waveguide-to-pillar coupling simulation result of the coupler fabricated in Section III. The simulated pillar is $150\mu\text{m}$ tall to better illustrate its effect. The simulated and experimental wavelength of light is 632.8nm . Twenty modes of equal power are launched in the waveguide and 79% of the input is observed at the top of the pillar. The power lost is due to the reflectivity of gold and light not being incident on the mirror or satisfying the total internal reflection condition at the pillar's sidewall. As the figure shows, the pillar confines the light and bends it at 90° . Polymer pillars are therefore flexible to substrate technology such that silicon can be used [13], [14], FR4 with imprinted silicon mirrors can be used, FR4 with a conventional 45° mirror can be used, and unwanted angular deviations due to the fabrication of a 45° mirror can be accounted for.

III. FABRICATION

A (100)-oriented silicon wafer is cleaned and a layer of SiO_2 is deposited on top using an STS plasma-enhanced-chemical-vapor-deposition (PECVD) tool. Photoresist is spun on and rectangular patterns are photolithographically defined to be transferred into silicon. A buffered oxide etch is then used to transfer the resist pattern into the oxide and an anisotropic etch in 25% tetra-methyl-ammonium-hydroxide at 85°C is used to transfer the pattern into silicon by etching along its (111) plane for a height of $19\mu\text{m}$. This etch reveals a 54.74° slanted sidewall that will be metallized to serve as the mirror. The remaining oxide is removed and $300/2000\text{\AA}$ of titanium/gold (Ti/Au) is selectively sputtered over the sidewalls, where Ti serves as an adhesion promoter. For the waveguide substrate cladding layer, $2\mu\text{m}$ of SiO_2 is deposited on the wafer using PECVD. Avatrel is

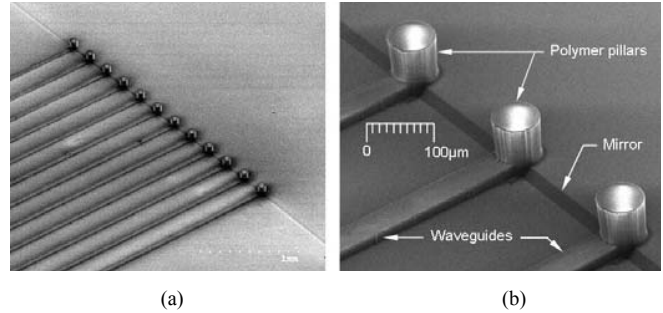


Figure 3. SEM images of an array of Avatrel waveguides (width = $40\mu\text{m}$, height = $15\mu\text{m}$), with Avatrel pillars (diameter = $75\mu\text{m}$, height = $58\mu\text{m}$) fabricated directly on top on a $250\mu\text{m}$ pitch, where (a) shows 12 pillars on mirror-terminated waveguide, and (b) shows a magnified image of (a).

spun on to a thickness of $15\mu\text{m}$. Channel waveguides are defined photolithographically to terminate at the mirror. Avatrel is again spun to a thickness of $58\mu\text{m}$ and the pillars are defined above the mirror-waveguide interfaces. The sample was cured at 200°C for 2 hours. Figure 3 shows SEM images of the fabricated coupler.

IV. OPTICAL TESTING

Waveguide-to-pillar coupling is first demonstrated using substrate-to-chip optical input interconnection. The experimental approach is to couple light into the multimode waveguide on the silicon substrate with a single-mode fiber and observe the light coupled into, and then out of, the pillar with a camera. Figure 4 shows the observed power that was coupled into the waveguide being coupled out of the pillar. The figure shows that mirrors can be used to couple light into polymer pillars and that once 54.74° mirrors are integrated with polymer pillars, the combination serves to produce a 90° bending of the light. An important message to note is that the pillars are tolerant to intentional and unintentional mirror-angle variations. Thus, if a 45° mirror is fabricated as a 48° mirror, the pillar will still produce a 90° bending of the light.

Pillar-to-waveguide coupling is next demonstrated. This represents chip-to-substrate optical output interconnection. The experimental approach is to couple light into the polymer pillar using a single-mode fiber and observe the light coupled into, then out of, the waveguide with a camera. The fiber has

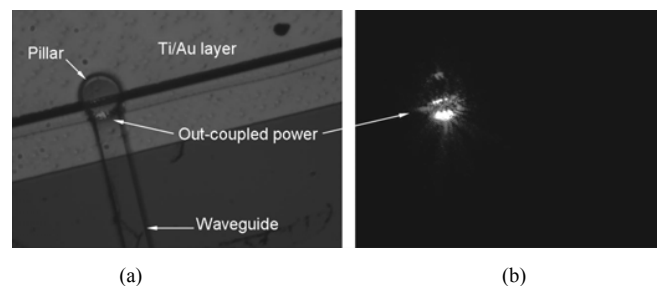


Figure 4. A mirror-terminated waveguide with a pillar on top as shown in Figure 3. A single-mode fiber (not shown) is used to couple light into the waveguide, and out-coupled power from the pillar is observed (a) with the camera light on and a 25ms exposure time and (b) with the camera light off and a 5s exposure time to see the effect of coupling.

a core diameter of $6\mu\text{m}$, and is used to simulate an equivalently sized VCSEL. Figure 5 shows the fiber residing directly on top of the pillar and coupling light into it, as well as light propagating inside the corresponding waveguide. Figure 6 shows the observed power coupled out at the waveguide end-face. These figures show that mirrors can be used to couple light from a polymer pillar into a waveguide.

V. CONCLUSIONS

Optical interconnects represent a potential solution to the bandwidth requirements for future GSI chips. To motivate their use, optical implementations must be compatible with electrical packaging and assembly requirements. To this end, polymer pillars have been developed as an I/O packaging technology. In this work, chip-to-substrate and substrate-to-chip optical interconnection were demonstrated using waveguides, mirrors

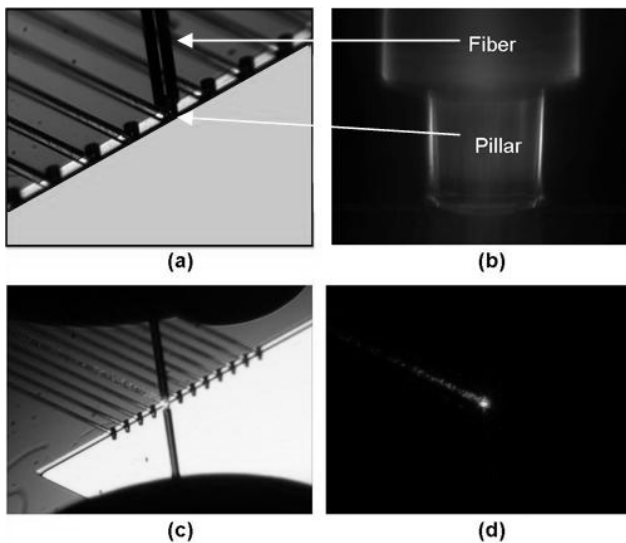


Figure 5. A fiber being used to couple light into a pillar and the resulting light coupled out of a mirror-terminated waveguide. (a) Shows an array of pillars-on-waveguides with a fiber directly on top of one pillar, (b) shows an in-plane image of the fiber on top of the pillar, (c) shows light being coupled into a pillar and then into a waveguide for an exposure time of 5 minutes, and (d) is the same image as (c), but with the camera light off and an exposure time of 1 minute, thus showing the light propagating inside of the waveguide.

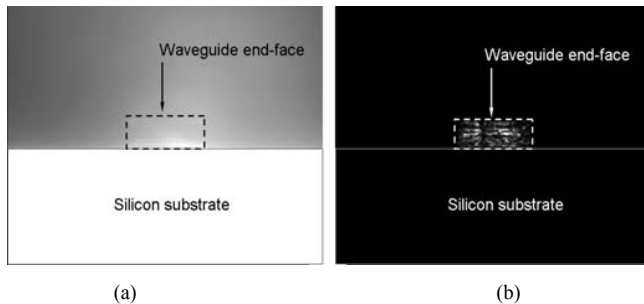


Figure 6. The end-face of the waveguide in the pillar-to-waveguide coupling measurement: (a) shows the waveguide end-face with the camera light on, and (b) shows the same picture as (a), but with the camera light off, laser light on and a 10ms exposure time – light is observed showing the light propagates to the end of the waveguide as expected.

and polymer pillars. The pillars were fabricated above the interface between metallized anisotropically-etched silicon sidewalls and the waveguides. Waveguide-to-pillar coupling was simulated to show that the pillar serves to produce a 90° bending of the light even without the use of a 45° mirror. The simulated efficiency was found to be 79% due to the reflectivity of gold and the light lost. Waveguide-to-pillar and pillar-to-waveguide coupling were experimentally demonstrated. Quantitative power measurements are now in progress. In conclusion, the waveguide-mirror-pillar configuration described herein was used to demonstrate a potential implementation of optical I/O interconnection for future GSI chip environments.

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