A Novel Via Blockage Model and Its Implications

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Abstract- Via blockage and its impact on wirability of multi-billion transistor chips are systematically analyzed. Along with a new via distribution based on a stochastic interconnect length distribution and on optimal multi-level interconnect network architecture, a physical via blockage model exploiting channel availability is proposed and applied to analyze future multi-level interconnect networks. This model reveals that the most severe via blockage occurs on first metal level, wasting more than 10% and up to about 50% of wiring area. A new perspective on chip size limit imposed by via blockage is also projected for future chips by using the proposed model.

I. Introduction

With increasing number of transistors on chip and shrinking minimum feature size, interconnects need to be considered from the very beginning of a design cycle. In determining available wiring area, design of multi-level interconnect architectures is sensitive to wiring efficiency [1,2] which accounts for wiring area consumed by power/clock networks and unused area [1]. The main reasons for unused wiring area are routing efficiency and via blockage [1,3,4]. Via blockage has been predicted to inhibit multi-level metalization [3]. A reasonable via blockage model is essential to fully understanding multi-level interconnect network design and performance. Such model also provides a quantitative means to characterize different CAD routing tools.

II. Via Distribution and Via Blockage Model

There are two types of vias on chip: *turn* vias and *terminal* vias. Turn vias appear out of routing necessity, connecting doglegs of interconnects. They are an internal part of interconnects, and therefore, do not add to the blockage caused by doglegs of interconnects. Terminal vias connect metal lines with silicon devices, and *do* create routing blockage at all intermediate levels. Consequently, only terminal vias are responsible for via blockage. Using only footprint area of vias to estimate their impact [5] is not sufficient because of ripple effect (Fig.1). When the number of vias is so large ("*dense vias*") that inter-via distance is less than average interconnect length, placing an interconnect must encounter a number of vias. Due to ripple effect, some potential wiring tracks, which are otherwise available as routing resources to routing tools, will be lost (Fig.2).

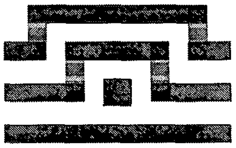

Figure 1. Ripple Effect of Via

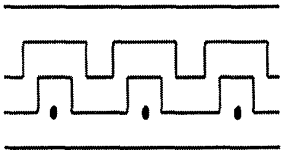

Figure 2. Wiring Track Availability Illustration

Therefore, a more realistic approximation of via blockage can be obtained by assessing wiring track availability in preference to footprint area.

By assuming 1) uniform placement of vias at every level, 2) use of X-Y orthogonal levels in pair, 3) placement of interconnects on appropriate levels exclusively based on length [2], 4) equally probable location of both terminals of an interconnect on either level of the same pair, and 5) grid mesh structure for power network [1,6,7] and negligible area for clock network [3,8], via distribution (N_v) in multi-level interconnect architecture can be found using a stochastic interconnect length distribution [9]:

For upper level of n-th wiring pair:

$$N_v = 2\left[I(L_{\max}) - I(L_n)\right] \qquad (1)$$

For lower level of n-th wiring pair:

$$N_v = 2I(L_{\max}) - I(L_n) - I(L_{n-1}) \qquad (2)$$

where $I(l)$ is cumulative interconnect density function [9], $L_{\max}$ is the longest interconnect length on chip in gate pitches, L_n is the longest interconnect on n-th pair. Then, the expression for via blockage factor, defined as the percentage of lost wiring area due to vias over chip area, at each level can be derived by calculating the frequency of lost wiring tracks due to vias (Fig.3):

$$B_v = \sqrt{\frac{N_v(2W)^2}{A_c}}\left(1 + \frac{s\lambda}{2W}\right) \qquad (3)$$

where A_c is chip area, W is metal width, s is via covering factor, and λ is layout rule unit. The novel via blockage model illustrates that smaller chip area, larger number of vias (which can be the result of larger chip complexity and bigger number of metal levels), and/or

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larger interconnect pitch leads to an increase in via blockage.

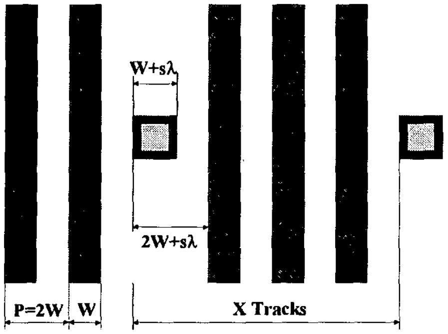

Figure 3. Via Blockage Factor Derivation

It is interesting to note that the via blockage factor in this novel model is exactly equal to the square root of the via blockage factor that would consider only footprint area of vias, which is appropriate only for "*sparse vias*". Given that via blockage factor is always less than unity, assessment based only on footprint area could substantially underestimate via blockage problems. The reason is the ripple effect of vias described above.

III. Case Study and Via-Limited Chip Size Prediction

This new model is applied to analyze via blockage in two multi-level interconnect network designs taken from [10] (Tab.1).

Table 1 Multi-level Interconnect Architecture Designs from [10]

Multi-tier Design: $A_c = 1.79cm^2$; Clock Frequency: f_c=2GHz				
Metal Level	M8/7	M6/5	M4/3	M2/1
Pitch, μm	1.78	0.94	0.45	0.2
L_n, gate pitch	7043	1862	887.7	209.6
Three-tier Design: $A_c = 0.70cm^2$; Clock Frequency: f_c=578MHz				
Metal Level	M8/7	M6/5	M4/3	M2/1
Pitch, μm	0.60	0.31	0.2	0.2
L_n, gate pitch	7043	1832	481	49.9

Number of vias at each level is calculated using via distribution model (Tab.2). As a figure of merit, the average interconnect length for each level is compared to the inter-via distance (Tab.3). Average interconnect length is determined first in *gate pitches*:

$$L_{avg} = \int_{L_{n-1}}^{L_n} l * i(l) dl / \left[I(L_n) - I(L_{n-1}) \right] \qquad (4)$$

where $i(l)$ is interconnect density function [9], and then converted to *interconnect pitch*. Comparison shows that an average interconnect can span from several to more than 100 vias which reaffirms that dense vias need to be dealt with in future chips. By assuming via covering factor equal to 3 [5], via blockage factor at each level is determined and shown in Fig.4.

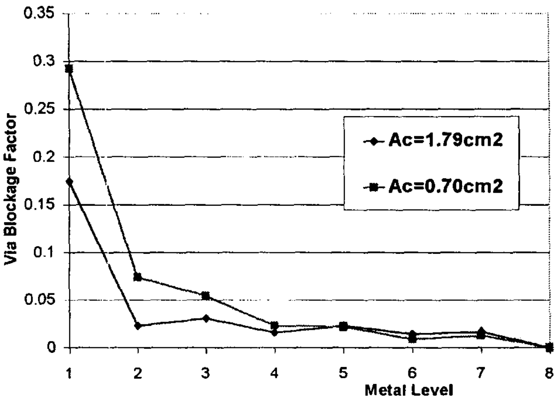

Figure 4. Via Blockage Factor at Each Level

It sends an important message that *via blockage is much higher at lower levels than at higher levels, and especially critical at the first level.* Note that the overwhelming portion of (short) interconnects and vias are placed at lower levels and the number of interconnects placed on a pair of levels decreases from bottom to top much faster than interconnect pitch increases.

Via blockage factors determined using the new proposed model are also compared to those obtained by using a methodology [11] based on [3] (Fig.5).

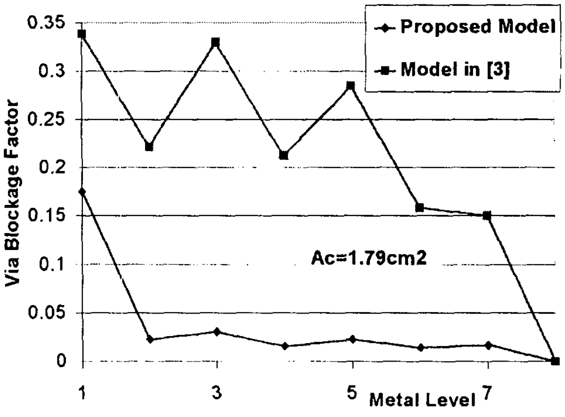

Figure 5. Model Comparison

While the previous via blockage model in [3] is concerned about number of metal levels and interconnect pitch *ratios*, the new proposed model additionally includes chip size and *absolute* interconnect pitch values into consideration. While the relative change in the number of interconnects on each level (thus in the number of vias) may be small when adding more levels, chip size shrinkage - the main benefit from more levels - can cause remarkable change in via blockage. Therefore, chip size should be considered as the direct cause for potential severe via blockage in future chips.

With further chip miniaturization, the first metal level that always has the most severe via blockage will become congested by vias earlier than any other level. Fig.3 suggests that it becomes impossible to route interconnects when inter-via distance is less than two in interconnect pitches. Based on this observation and worst case estimate for the number of vias:

$$N_{v,\max} = 2I(L_{\max}); \quad I(L_{\max}) = \alpha k N(1 - N^{p-1}) \quad [12] \quad (5)$$

where N is number of gates, k is Rent's coefficient, p is Rent's exponent, and α is a factor determined by fan-out (their values are taken from [10]), via-limited chip size ($D_{\min}$) is determined for future chip generations projected by [13]:

$$D_{\min} = \left(A_{eff} / A_c\right)^{-1}(4W + s\lambda)\sqrt{2\alpha k N\left(1 - N^{p-1}\right)} \quad (6)$$

where A_{eff} is wiring area left by power supply network, and assumed to be around $0.8 * A_c$ [3,7]. It is compared with gate-limited chip size:

$$D_{gate-\lim ited} = \sqrt{N(\beta F^2)} \quad (7)$$

where β is a numerical factor, F is minimum feature size. With compact gate design, via limit is to be hit first in chip miniaturization by using multi-level metalization (Fig.6).

IV. Conclusion

A physical model of via blockage that is built upon a stochastic interconnect length distribution and a multi-level interconnect network incorporates chip size, number of transistors, performance requirements (through interconnect pitches), and Rent's parameters. This new model reveals that the via blockage factor on the first metal level is as high as 10% to about 50%, while via blockage at higher levels is much smaller. It appears that the via blockage on the first metal level is the prime determinant of wiring limited chip size in the future.

Acknowledgements

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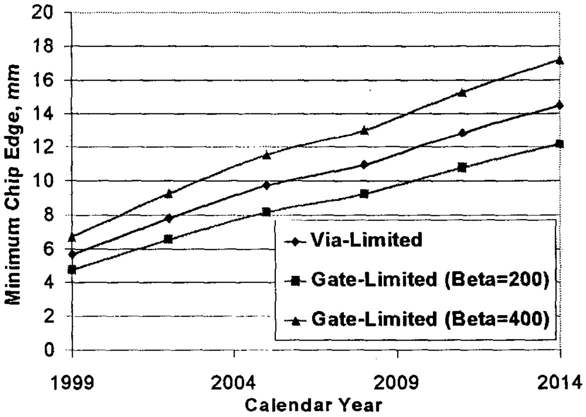

Figure 6. Via-Limited versus Gate-Limited Chip Size

Table 2. Number of Vias on Each Level

Metal Level	M8	M7	M6	M5	M4	M3	M2	M1
N_v (A_c=1.79cm^2)	0	$1.45*10^4$	$2.90*10^4$	$7.74*10^4$	$1.26*10^5$	$4.40*10^5$	$7.55*10^5$	$3.76*10^7$
N_v (A_c=0.70cm^2)	0	$1.51*10^4$	$3.02*10^4$	$1.63*10^5$	$2.96*10^5$	$1.61*10^6$	$2.93*10^6$	$3.86*10^7$

Table 3. Inter-via Distance versus Average Interconnect Length

	Metal Level	M8	M7	M6	M5	M4	M3	M2	M1
Ac=1.79cm^2	Via Distance, interconnect pitch	N/A	50	67	41	67	36	63	8
	L_{avg}, interconnect pitch	5425		5013		3379		145	
Ac=0.70cm^2	Via Distance, interconnect pitch	N/A	91	124	53	61	26	20	5
	L_{avg}, interconnect pitch	9951		6554		1592		59	