Wafer-Level Microfluidic Cooling Interconnects for GSI

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Abstract

We present a novel CMOS compatible approach to fabricate on-chip microfluidic cooling channels using a spin-on sacrificial polymer material at wafer level. Deep trenches (>100μm) etched into the backside of an IC wafer were successfully filled up by a single spin coating step with a high viscosity sacrificial polymer. A porous overcoat material allows the decomposition of the polymer to form enclosed microchannels. Through chip holes and polymer pipes are used as the inlet/outlet interconnects. Different channel array designs were described and the pressure drop was estimated for a heat flux of 100W/cm^2 with DI water flow rate. The resulting cooling scheme offers a simple and compact solution to transfer cooling liquid directly into a GSI chip and is fully compatible with flip-chip packaging.

I. Introduction

Reliability and performance of interconnects are heavily dependent on their operating temperature. Therefore, chip cooling is critical for advanced ICs as the power density increases continuously. According to the ITRS, the power density will reach 100W/cm^2 for the high performance applications in 2018, and there is no manufacturable solution to remove such a high heat flux with conventional IC packaging technologies [1]. Moreover, 3D microsystem integration raises even more significant challenges in thermal management. While tremendous research is being conducted on improving thermal interface materials [2-4], microfluidic cooling has been considered as an ultimate solution to these issues for decades [5,6]. For instance, Tuckerman demonstrated a power dissipation capability of 600W/cm^2 with a water flow of 10cm^3/s in 1981 [5]. Unfortunately, the conventional microchannel fabrication methods require wafer bonding process, which usually needs high temperature, and/or high voltage, vacuum operation, and additional cost for the cover wafer. These approaches are not likely to be adopted in the standard BEOL manufacturing facilities and a feasible chip-scale microfluidic cooling scheme is yet to be implemented.

In this work, a CMOS compatible approach is proposed to fabricate on-chip microfluidic cooling channels. Process integration with flip chip packaging is described and material selection and trench filling are also investigated. Combined with through chip inlet/outlet holes and compliant heat pipes [7], the microchannels on the backside of an IC chip can be used to circulate the cooling liquid from a PWB substrate with embedded microfluidic channels.

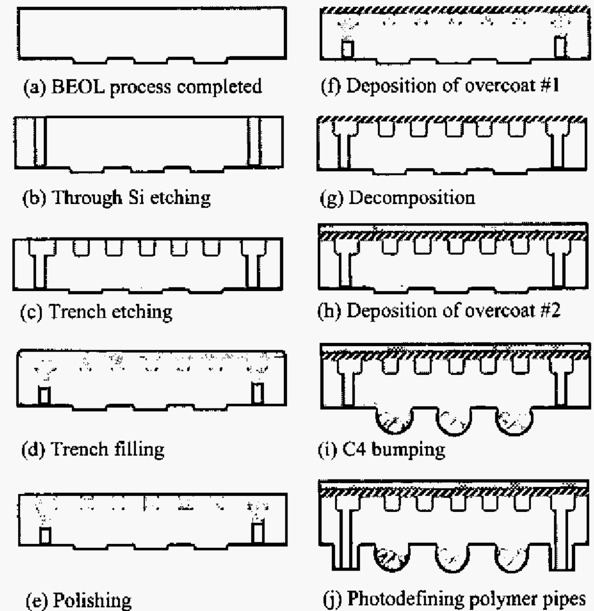

Figure 1. Schematic illustration of monolithic fabrication of on-chip microfluidic cooling interconnects for flip-chip packages

II. Process Integration of On-chip Microfluidic Cooling Interconnects for a Flip Chip

Fig.1 shows the schematic of fabrication process of microfluidic cooling channels for a flip chip. The process begins following the BEOL process (Fig.1a). The through wafer holes and deep trenches are first etched from the backside of a wafer using the Bosch process in an ICP-RIE as shown in Fig.1b and Fig.1c. A sacrificial polymer material is then spun on to fill up the deep trenches. Due to planarization effect, the surface of the wafer backside can be covered (Fig.1d). After softbake, the wafer is polished for a short time to remove the extra sacrificial polymer (Fig.1e). Then a layer of porous overcoat is first deposited (Fig.1f). To decompose the sacrificial polymer, the wafer can be heated up in an oven with controlled ramp rate (Fig.1g). Once the sacrificial polymer is completely removed, the enclosed microfluidic channels are formed. To enhance its mechanical strength and sealing, a second layer of overcoat can be applied as shown in Fig.1h. The enhancing overcoat may be a spin-on polymer layer, a high quality SiO_2 thin film, or an electroplated metal sheet. The wafer is then bumped with a standard C4 process (Fig.1i). Finally, the

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wafer is flipped and a thick layer of photoimageable polymer can be used to fabricate the fluidic pipes onto the front side of the wafer [7]. The polymer pipes should be aligned with the inlet/outlet holes and the passivation layer inside the pipes are then etched to allow fluidic circulation (Fig.1k).

After cleaning and drying process, the wafer is ready for dicing. The resulting flip chip can be mounted onto a liquid-cooled PWB substrate, which is equipped with embedded microfluidic channels and powered by integrated or external pumps for liquid circulation. The conventional underfill may be utilized to achieve hermetic sealing.

III. Materials Selection and Processing Condition

The two key elements in microfluidic channel fabrication include the sacrificial materials and the overcoat materials. Since the target depth of the Si trenches is large (> 100μm), sacrificial materials and spin coating condition need to be carefully selected to achieve optimal filling effect. Two formulas of the sacrificial polymer (Unity 200, Promerus, LLC.) were experimented. One is the low viscosity type (LV), and the other is the high viscosity (HV) type.

Figure 2 shows the cross-sectional SEM images for the deep trenches after filling with two types of sacrificial materials. LV polymer shows a poor trench filling effect. Even with a slow spin speed (800rpm), the 100μm deep trenches can only be filled by 20% after three spin steps using LV material. In contrast, with the HV material, the trenches can be covered by nearly 100% after only 1 spin step at 1500rpm.

(a) LV sacrificial polymer (3 spins at 800rpm) (b) HV sacrificial polymer (1 spin at 1500rpm)

Figure 2. Cross-sectional SEM images of the deep trenches after filling with different sacrificial polymer materials

The spin coating process not only fills up the trenches but also builds up an extra layer of the polymer on the wafer surface due to the high viscosity. The thickness of the extra polymer film was about ~15μm above the Si surface, which can be easily removed by mechanical polishing. Fig.3 illustrates a filled deep trench after polishing for a short time. The build-up film was removed and a smooth Si surface was exposed. In some area, the sacrificial polymer inside the trenches was slightly damaged due to the manual operation. This problem can be avoided when a precision polishing tool is used in the future. To form enclosed microfluidic channels, a porous overcoat is required to allow permeation of the gaseous products resulted from the decomposition process. In the preliminary experiments, a porous SiO_2 thin film (~2μm) was first deposited with PECVD at 150°C and a layer of polymer (Avatrel 2000P, ~10μm) was then spin-coated and cured. Fig.4 shows cross-section of a completed microchannel. As expected, the sacrificial polymer inside the trenches was completely removed by heat treatment in a N_2 purged oven at a controlled ramp rate and low temperature (<300°C).

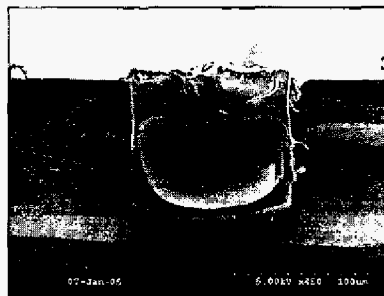


Figure 3. Perspective view of a filled deep trench after mechanical polishing: the extra polymer is removed and the Si surface is exposed

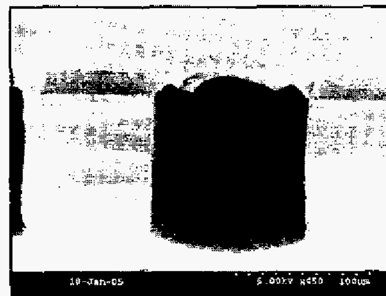


Figure 4. Cross-sectional SEM image of an enclosed microfluidic channel

IV. Channel Array Design and Pressure Drop

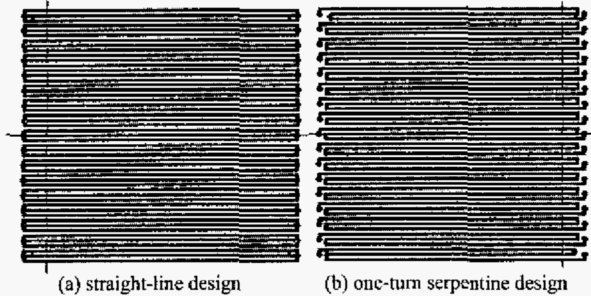
Two different designs of on-chip microfluidic cooling channels were investigated for a 1cm×1cm chip area, as shown in Fig.5. Design 1 has 51 parallel channels and every three channels share a pair of inlet/outlet holes (Fig.5a). In design 2, the channels are in an one-turn serpentine shape to achieve a more uniform temperature gradient (Fig.5b). The opening of the through Si holes is well aligned with the micro channels as shown in Fig.6.

Since the overall heat-exchange area is identical for the two designs, their heat removal capability is the same for a given overall flow rate of any cooling liquid. To remove a heat flux of 100W/cm^2 with DI water, the minimum overall flow rate of 0.4cc/s is required for a temperature difference of 60°C between the inlets and outlets. Meanwhile, the pressure drop between an inlet and an outlet can be estimated according to the empirical equation of fluidic mechanics [6,8]:

$$\Delta P = 32 \times L \times \mu \times \frac{V}{D_h^2} \qquad (1)$$

where L is the channel length; V is the water flow velocity determined by the mass flow rate; μ is the viscosity of water;

and the D_h is hydraulic diameter. Figure 7 plots the calculated pressure drop between an inlet and an outlet as a function of the channel depth with a channel width of 100μm for the two channel array designs. Pressure drop on a single channel decreases as the channel depth increases. It is due to the increase of channel cross-section area and the decrease of fluidic velocity accordingly.



(a) straight-line design (b) one-turn serpentine design

Figure 5. Two types of channel array design for a $1cm^2$ chip area

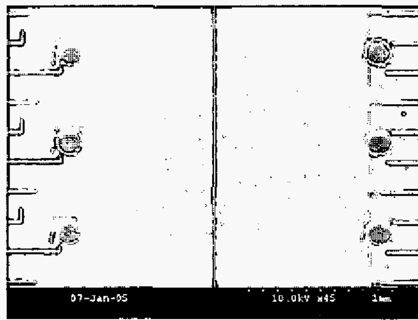


Figure 6. SEM image of the through Si holes as the inlets/outlets aligned with the micro channels

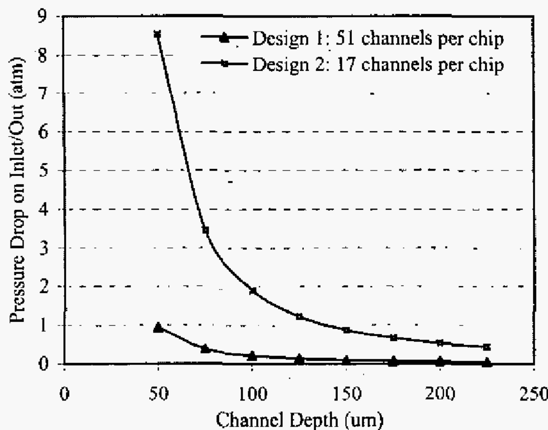


Figure7. Pressure drop between an inlet and an outlet for the two types of channel array (channel width: 100μm; heat flux: $100W/cm^2$)

The magnitude of pressure drop required for a channel in the design 1 is small and comparable to that in literature [6] with the same channel length of 1cm. Thus, a small channel depth can be used for the design 1. A channel in the design 2 requires a higher pressure drop because of its longer channel length. A channel as deep as 100μm is needed to reduce its pressure drop below 2 atms, which is a feasible value with an external water pump or the state-of-art integrated micropump technologies [9].

V. Conclusion

Thermal management of high power density IC and 3D integration calls for on-chip microfluidic cooling. We presented a compact scheme to transfer the cooling liquid directly to a chip to eliminate the thermal interface material issues and effectively remove high heat flux at low cost. A CMOS compatible process was developed to fabricate the on-chip microfluidic cooling channel using a sacrificial polymer and layered overcoat materials. Two channel array designs were proposed with multiple inlet/outlets. Pressure drop requirement was estimated for various channel depth. Our ongoing work includes hermetic assembly of test chips with on-chip microchannels onto the PWB substrate with embedded fluidic channels. We expect to remove a heat flux of $100W/cm^2$ with pressure drop less than 2 atms.

Acknowledgements

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