

BIOLOGICAL LEARNING MODELED IN AN ADAPTIVE FLOATING-GATE SYSTEM

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ABSTRACT

We have implemented an aspect of learning and memory in the nervous system using analog electronics. Using a simple synaptic circuit we realize networks with Hebbian type adaptation rules. With increased synaptic activity, the synaptic weights are increased or decreased. That increase or decrease continues with subsequent synaptic activity. This paper explores the relationship between synaptic activity and weight for various inputs

We will use our relatively simple network to bootstrap into larger, more complex systems. This system helps to provide insight into intricate natural designs, such as cerebellar cortex. Using the physical properties of our floating-gate pFET device, we are able to re-establish properties seen previously and build upon these first steps [1], [2]. We can modify our learning rule rates and dynamics through capacitively coupled input voltages. Our learning rule has connections to reinforced learning, and therefore may find useful engineering applications [3].

We define action-potential networks as networks where the inputs (X) and outputs (Y) take on binary values (0 or 1) for a short period of time, analogous to action-potentials. Information is encoded in the relative arrival of information. These networks result in binary decisions of important regions of activity; therefore, we can selectively turn on adaptation during these phases of operation. We use the term *action-potential signals*, to differentiate between nodes that were primarily intended for rate-encoded signals.

Correlations between signals are also key to learning and memory. Input to a neuron must reach a threshold before that neuron fires an action potential. Often, multiple inputs are needed to create an action potential [4],[5]. These inputs from different neurons must act collectively in order to produce an effect. Thus, the output is also determined by the interaction between inputs. Our action-potential network depends on the relationship between inputs as well.

I. PREVIOUS WORK

Our research is motivated by three key issues. First, we wanted a dense floating-gate synapse that can be used in action-potential based networks. Our approach is based upon single-transistor learning synapses (STLS) and in the resulting dynamics of nFET and pFET based synapse elements [1], [2]. The STLS embodies the five properties of a synapse: storage, multiplication, outer-product correlation, small size, and low-power consumption. Large on-chip arrays are possible since these elements are the size of 2 to 3 EEPROM cells. Approaches based upon large floating-gate circuits for each synapse may provide some interesting phenomena at a small scale [6], but rarely will they scale to large problems, such as investigating networks of thousands of units.

Second, we will base our neuron circuit on pFET floating-gate devices. Hebbian-type adaptation has been seen in simple coupled networks of pFET devices [2]. Furthermore, pFET hot-electron injection, the primary adaptation mechanism in STLS, directly scales with current digital CMOS processes, and can not be eliminated without radically affecting basic MOS-FET performance. Previous reports were based on nFET devices, but these devices have only worked in a 2.0 μ m BiCMOS process [7].

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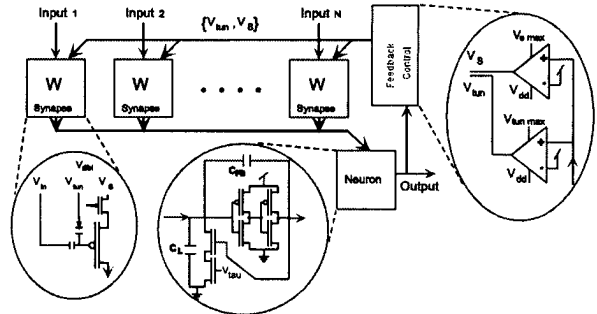


Fig. 1. Basic floating-gate circuit for an action-potential learning system. Our synapses are a single floating-gate pFET device with a DIBL transistor for stability. The neuron element is an integrate and fire neuron that can be easily modified to more biological neuron models. The feedback circuitry moves the source (V_s) and tunneling (V_{tun}) voltages after the onset of an action potential. The current from each synapse is summed along a wire; extending this circuit to biological type dendrites would be straightforward.

Third, we desire a system using STLS circuits to show behaviors involving correlations between at least two inputs. Only recently have results shown correlation effects in adaptive floating-gate elements [8], [9], [10]. Earlier work did not address the interaction of two or more inputs results in behavior not seen in zeroth order characterization of a single device, even if in a network [7]. Placing this work in a biologically plausible environment leads to many open questions which this work will address. Here, our primary goal is to explore learning in a biological environment, not signal-processing applications.

II. THE FLOATING-GATE ADAPTIVE CIRCUIT

Figure 1 shows the schematic for our action-potential based learning network. Our circuit has three main components: a floating gate array, an integrate and fire neuron, and a feedback circuit that enables adaptation and therefore the learning rule. Each synapse element is a single pFET floating-gate transistor, or single transistor learning synapse (STLS). The dendrite, the connection between the synapses and the neuron, is currently a wire, but it could be implemented using silicon models of dendrites [11], [12].

The floating-gate array acts like a conglomerate of synapses. As the input to a STLS becomes stronger (further below V_{dd}), the system increases the strength of that synapse. The synapse strength decreases as the input to that unit weakens. Synaptic strength is represented as the charge on the floating gate, which defines the synapses' weight. Since pFET floating gate elements are used, the weight is directly related to both the charge on the gate and current through the FET.

The integrate and fire neuron circuit approximates the basic function of a neuron; it sends a digital spike (action-potential) after a threshold has been reached by the input signal [13]. This circuit can be seen as a current-to-frequency converter. The frequencies used are in the range of sub-Hz to 1 kHz. This neuron model could be replaced with other models in a

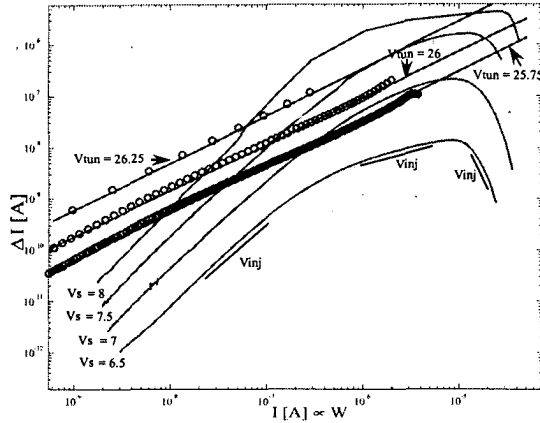


Fig. 2. Experimental measurements of electron tunneling and hot-electron-injection rates of our pFET floating-gate synapses built in a 1.2 μm process. These measurements were taken in a manner similar their use in the adaptive network: the currents are measured at their non-injecting state, and then briefly returned to their adapting state. The power supply and tunneling supply are set to 5 V when not adapting. The resulting power-law for the tunneling curves is roughly 1, while the resulting power-law for the injection curves is varies from 2 to -3. This decrease in the injection exponent is the result of devices injecting at above-threshold currents due to capacitive coupling. The capacitive coupling associated with modifying the tunneling and injection voltages will decrease both the injection and tunneling rates, but the injection rate is still larger than the tunneling rate for a wide-range of parameters. This coupling will shift these curves during operation resulting in different equilibrium points.

straightforward manner; the network properties will be dependent on the type of model used [14]. More accurate neuron models will allow the system to act more like natural neurons.

The feedback circuit connects the neuron back to the synapse array. When the neuron fires, the feedback circuit increases the weights of synapses with input and decreases the weights of synapses without input. The rate at which the weights grow or shrink depends on the dynamics of the action-potential pattern coming from the neuron. If there is no input from the neuron, the weights will remain the same. Input to the feedback section increases both the tunneling and injection voltages, allowing synaptic adaptation.

The inputs are digital signals equivalent to action-potentials. These experiments used action-potentials 1 ms in length. The outputs come from an integrate-and-fire neuron, as seen in Fig. 1.

III. THE ADAPTIVE LEARNING RULE

We define a learning rule such that learning only occurs when a neuron fires an action potential. We use output action-potentials to define when to adapt the weights, as proposed elsewhere [6]. During normal operation the node has three states, as illustrated in Table I. When the output is equal to zero ($Y = 0$), no learning occurs. This effect is directly achieved by turning off all floating-gate currents. When the output is equal to one ($Y = 1$), then two weight updates are possible at each synapse. If a synapse received an action potential ($X = 1$), then that device has some channel current, resulting in hot-electron injection currents. This effect will increase that synapses' weight unless the weight is too small. When the weight is very low, electron tunneling dominates the process. If a synapse received no action potential ($X = 0$), then there is no channel current, eliminating hot-electron injection currents, resulting in the weight decaying towards 0.

III-A. Inherent Learning Rule

By only turning on adaptation as a result of an action potential, we use circuitry to move the tunneling and source voltages for a fixed duration after the onset of this action-potential. We use hot-electron injection and

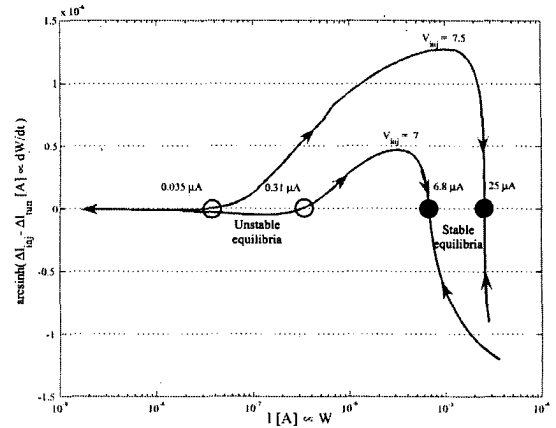


Fig. 3. State-space analysis of learning rule. Two cases of simultaneous tunneling and injection are explored. As illustrated, we can shift our equilibrium points to desired locations by varying the tunneling and injection voltages. Furthermore, the trajectories of the weights can be determined for a given initial condition. The arcsin function is used to magnify the detail of the data.

Table I. $\tau \frac{dW}{dt}$ for various cases

	No Input $X=0$	Input $X=1$
No Output $Y=0$	0	0
Output $Y=1$	$-W^{1+\beta}$	$W^{1+\alpha} - W^{1+\beta}$ $\approx W^{1+\alpha}$

electron tunneling to bidirectionally increase or decrease the strength of the STLS [1],[2]. Hot electron injection is often the primary adaptation mechanism since the resulting weight change is a product of its input signal (gate terminal) and corresponding error signal (drain voltage).

The tunneling voltage and power-supply voltage are capacitively connected to the floating-gate, therefore the current that the circuit operates at is only a monotonic function of the current level used during adaptation. We could reduce this effect by using a capacitor compensation scheme during the adaptation phase, as done elsewhere [15]. We may inject at above threshold currents due to this capacitive coupling. This effect would cause our V_{inj} slopes to change and allow for greater flexibility in the learning rule. Although a strong dependence was expected between the gate and the current, the tunneling junction provided an unexpectedly high dependence as well. This relatively high value of κ forces us to re-evaluate our circuits and learning rule. As stated earlier, the feedback block determines the voltage of the tunneling junction. The pulses from the feedback circuitry may produce large enough currents to cause the circuit to run in the above-threshold state. The learning rule described above holds true in above-threshold operation of the transistors, with modified values of α and β as seen in Fig. 2. The same is true for the injection node, however, this coupling ratio is small and should not drive the circuit in to the above-threshold state.

To model the behavior of the floating-gate synapse during an action potential, we start from a combined model of tunneling and hot-electron injection as [2]

$$Y = 1 : \tau \frac{dW}{dt} = XW^{1+\alpha} - W^{1+\beta},$$

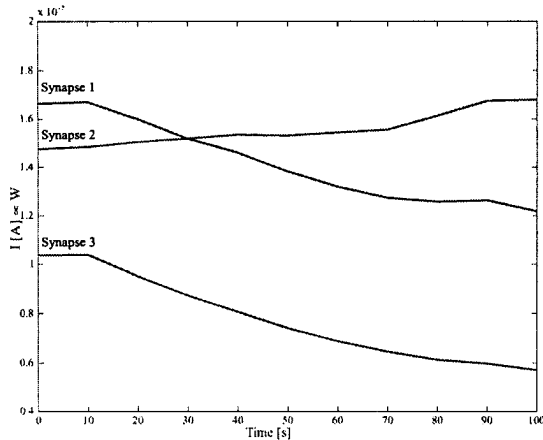


Fig. 4. Experimental measurements from 3 synapse system, where one synaptic input (Synapse 2) is visited significantly more than the remaining 2 inputs. Weight adaptation at a particular synapse is dependent upon the occurrence of input pulses with output pulses. With an increase in synaptic activity, the probability of input and output pulse-overlap also increases. The overall network adaptation rate is dependent upon the tunneling and injection voltages. We illustrate the case where we have a combination of LTP and LTD occurring in the system.

$$\mathbf{Y} = 0 : \frac{dW}{dt} = 0, \quad (1)$$

where W is the weight of the synapse due to slow changes in the floating-gate charge, X is a binary variable designating whether an action potential was input, $\tau = \frac{C_T U_T}{\kappa I_{tun0}}$, $\alpha = 1 - \frac{U_T}{V_{inj}}$, and $\beta = \frac{U_T}{\kappa_p V_g}$. Typically, β is greater than, but nearly equal to, 0, where α is typically between 0 and 1 [2]. The term C_T is the total capacitance at the floating gate node, U_T is the thermal voltage, and I_{tun0} is the baseline tunneling current.

From Fig. 2, we see measured data from our 1.2 μ m chip of $\frac{dW}{dt}$ versus W when only injection current is present (no tunneling current) and when only tunneling current is present (no injection current). When tunneling and injection currents are equal, we get an equilibrium weight (W_{eq}), which is typically an unstable point for pFET floating-gate devices [2]. If W is above W_{eq} , we have a Hebbian type learning rule, but if W is below W_{eq} , the weight always decreases towards zero. This learning rule is one natural form of weight pruning; however, this algorithm could be a problem if we want to reuse this synapse.

Figure 2 shows some intriguing dynamics from this 1.2 μ m chip because α , the power-law for the injection dependence, becomes less than the electron tunneling dependence. This result implies there is an expanded region of operation where this floating-gate element will converge to an equilibrium point, rather than rapidly diverging to one of the power supply rails. This convergence upon a particular equilibrium point that we can set is further illustrated in Fig. 3. We are not using the DIBL FETs for source-degenerated pFET floating gates so that we can preserve these Hebbian-like instabilities.

III-B. Tuning Dynamics

When α and β of (1) are tuned such that injection is the dominant term, the entire system exhibits effects similar to LTP and LTD when tunneling is the dominant term, as eluded to earlier. We can combine these effects to modify our learning rule. As seen from Fig. 2 the values of α and β can be altered by the values of V_{inj} and V_{tun} . Note that V_{fg} is the voltage at the floating gate node. When there is no feedback, V_{tun} and V_{inj} are set to V_{ad} , effectively turning tunneling and injection off. Input to a synapse lowers the V_{fg} . This lower V_{fg} causes a larger difference between V_{fg} and V_{tun} and between V_{fg} and V_{inj} , thus increasing the effects of tun-

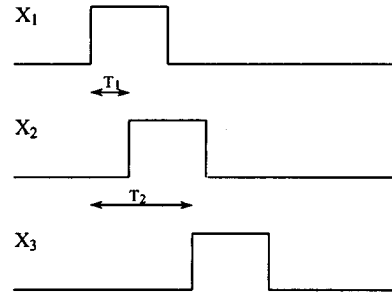


Fig. 5. Illustrates the concept of delayed inputs to synapses, where X_n is the input to *synapse_n* and T_n is the delay between *synapse₁* and *synapse_{n+1}*.

neling and injection on that particular floating gate as compared to other floating gates in the array.

IV. SINGLE INPUT EXPERIMENTS

One might initially ask what happens when a single input is held low (and therefore an event), while all the other inputs are held high (and therefore no event). This test is much like the biological experiments which explored the existence of LTP [4]. In this case, we experimentally see in Fig. 4 that selected synapse will diverge towards larger currents, while the other synapses diverge towards zero. This result is not surprising. From previous results, we would expect a single synapse to act if it were basically isolated and the remainder to also act isolated [2]. Thus, we have a scheme that is reminiscent of Hebbian learning.

V. CORRELATION EXPERIMENTS

Although our previous experiments explore networks of STLS, they do not encompass the effects of overlapping inputs. In biology, simultaneous inputs are often needed to elicit a response. For instance, for LTP to occur, both a constant signal from one input and a strong input are needed to strengthen the synapse [4].

We present another experiment which further explores the dynamics of our system. Here, the inter-synapse effect is the main focus. This scheme involves overlapping input pulses in time to determine the effect on the system as shown in Fig. 5. Like the previous experiments, the input pulse widths should be 1 ms long. The amount of overlap, number of synapses receiving input, and pattern of input are the main parameters of this set of experiments. In a living neural network, the system output often depends on the sequence of inputs and the interaction between individual neurons within that network. Thus, this experiment allows a more realistic view into the system's behavior.

For instance, if the standard pulse is short enough, the feedback from the first and third synapses should strengthen the second synapse more than the first or third, due to the fact that the second synapse has input in enough time to receive the feedback from itself, the first, and the third synapse. The first synapse would not gain any benefit of feedback from the third since it is off by the time the third is on. However, the third could receive feedback from the first if T_2 is short enough. Both the first and third synapses would receive feedback due to the second synapse.

Experiments involving changing the duration of this standard pulse will provide further insight on how the synapses affect each other. Experiments involve randomly sending inputs to all synapses, randomly sending inputs to all synapses while emphasizing two much more than the others, varying the rate of tunneling, and varying the rate of injection.

VI. CONCLUSION

This work successfully produces learning and memory in silicon. Recognizing the specifications for creating neural networks on chip, the central circuit of the design is the STLS. A network, including an array of STLSs, a simple neuron model, and feedback, was implemented. Although this initial network was small, essential insight on the behavior of a STLS network has been gained. It was discovered that the STLS network exudes a

learning rule which is quite similar to what is found in biological neural networks. Main attributes of the STLS network are LTP like behavior (a Hebbian learning rule) and its compliment LTD.

VII. REFERENCES

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