An Exponential Model of Channel-length Modulation Applied Towards Floating-gate Circuits

Chris Duffy, Matt Kucic, AiChen Low, and Paul Hasler
Georgia Institute of Technology
Atlanta, GA 30332
cjduffy@ece.gatech.edu, q@gatech.edu, lowa@ece.gatech.edu, phasler@ece.gatech.edu

Abstract — Modeling of the drain current-voltage relationship often is the primary effect that limits the performance of floating-gate circuits. In this paper, we propose and discuss a model of drain-voltage effects (such as channel-length modulation) on channel current based upon a novel use of an exponential dependence of drain voltage. This exponential formulation cleanly models the MOSFET behavior throughout the spectrum of long and short channel devices. This exponential formulation also simplifies the solution of basic amplifier circuits, and gives some suprising results of the linearity of two-transistor amplifiers. This exponential formulation is consistent with the effects seen due to floating-gate to drain capacitance in floating-gate circuits.

I. Purpose and origins of this model

This discussion focuses on the subthreshold region of MOSFET operation. As devices scale power supplies are reduced; consequently, the subthreshold regime becomes a larger part of our available input range. It also allows lower drain-to-source voltages while remaining saturated. Hence, operation in subthreshold is especially desirable for low-power applications. In addition, the transconductance gain (g_m) of a subthreshold MOSFET is comparable to that of a BJT (for equivalent bias currents).

If we can utilize MOSFET devices at process capability, then the shorter transistors will give us increased current levels and transconductance per unit area. In other words, for a constant MOSFET width-to-length ratio, using shorter channel lengths allows us to scale down our devices, which costs less die area and less unwanted parasitic capacitance. We present a model that adequately describes the dependence of drain current on drain voltage for short-channel MOSFETs, but is nevertheless easy to use.

This model was inspired by the exponential dependence of drain current upon drain voltage in a floating-gate transistor as shown in Fig. 1. As the drain voltage of the floating gate is moved below the well potential (i.e. V_d is increased), the gate voltage is lowered for a fixed V_{in} due to the overlap capacitance C_{gd}. Hence, an increasing V_d results in a substantial current increase, which can be viewed as a reduction of the threshold voltage. We model

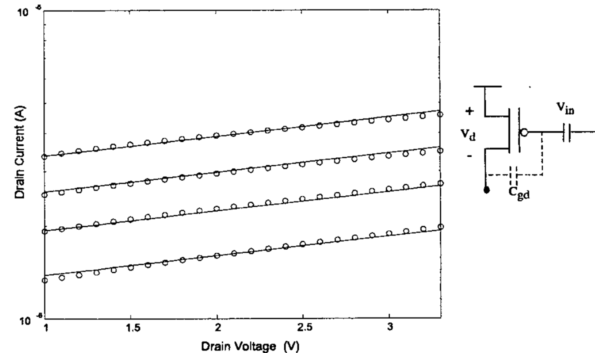

Fig. 1. Drain current versus drain voltage of a floating-gate pFET at four gate voltages. Since the floating-gate is capacitively coupled to the drain voltage through C_{gd}, moving the drain voltage below the bulk reduces the threshold voltage of the device. The experimental data are fitted to $I = I_{bias}e^{\Delta V_d/V_{A,eff}}$, where $V_{A,eff} = 6.92V$ and I_{bias} is a curve-specific offset.

this effect as

$$I = I_{bias}e^{(\kappa C_{gd}\Delta V_d)/(C_T U_T)} = I_{bias}e^{\Delta V_d/V_{A,eff}}, \quad (1)$$

where C_T is the total capacitance at the floating gate, I_{bias} is the large-signal drain current (set by the floating-gate's initial value), κ is a fraction (< 1) representing the capacitive coupling of the gate to the channel, U_T is the thermal voltage, and $V_{A,eff}$ is the effective Early voltage of the floating gate device. (Remember that the low value of $V_{A,eff}$ is due to capacitive coupling – there are *no* short-channel effects evident in this example.) It will soon become evident that we do not restrict our use of the parameter V_A to describe a single physical phenomena (such as channel-length modulation); rather, our use encompasses several effects that result in the dependence of a MOSFET's channel current upon its drain voltage.

II. The MOSFET relationship of channel current versus drain voltage

When a subthreshold MOSFET saturates (at approximately $V_{ds} > 4U_T$), we model the current through the

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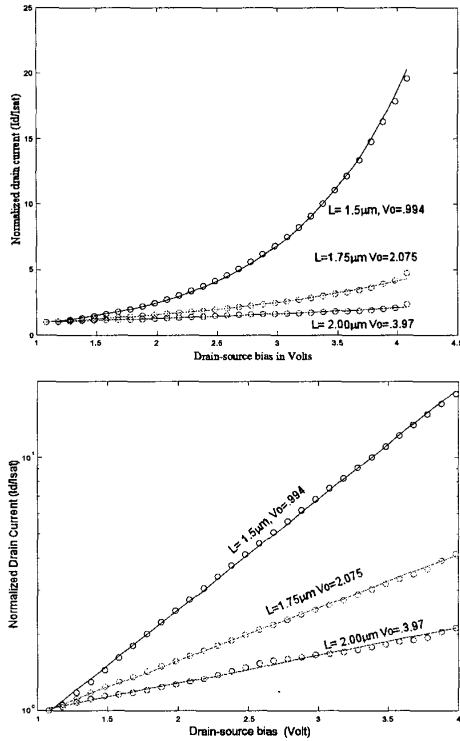

Fig. 2. Empirical measurements of drain current versus drain voltage for three different channel-length nFETs in a 2.0 μm process at a gate voltage 0.518V above substrate. In the top plot, the linear scale shows that the drain current's dependence upon V_{ds} is strong and nonlinear for devices shorter than minimum length. On a logarithmic current scale (the bottom plot), straight lines validate an exponential representation of drain current versus drain voltage.

channel, based on [1] as

$$I = I_o(e^{(\kappa V_g - V_s)/U_T})e^{V_{ds}/V_A} = I_{sat}e^{V_{ds}/V_A}, \quad (2)$$

where I_o is analogous to the reverse saturation current in a BJT, and I_{sat} is the ideal drain current in saturation, assuming no dependence on drain voltage. Fig. 2 shows that real devices can show a significant drain-voltage dependence. The effect of the drain voltage modulating the channel's length is known as channel-length modulation or the Early effect, where V_A $(=1/\lambda)$ is the Early voltage. Although we will focus on MOSFETs, we could similarly express the collector current in a BJT as

$$I = I_o e^{(V_b - V_e)/U_T} e^{(V_c - V_e)/V_A}. \quad (3)$$

The lowest curve in both parts of Fig. 2 shows drain current versus drain voltage for a MOSFET with the minimum channel length allowed by the process' design rules. The weak dependence of its channel current on drain voltage is adequately described by the classic model of the

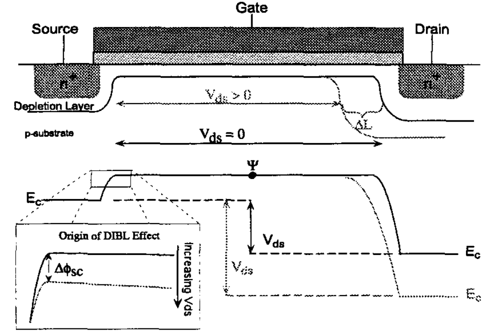

Fig. 3. Cross section and energy band diagram of a MOSFET. As V_{ds} increases, the channel grows shorter; therefore, the current increases. Also, a drop in electron potential at the drain of an nFET induces a small drop in the electron potential of the channel at the source-channel interface. (The picture of the source barrier is enlarged.) The current density through the channel increases as an exponential function of the source barrier reduction.

Early effect:

$$I = I_{sat}(1 + \frac{V_d}{V_A}) \Rightarrow \frac{\Delta I}{\Delta V_d} = \frac{I}{V_A}. \quad (4)$$

Unfortunately, this classic model does not adequately describe the drain voltage dependence when the channel length is reduced below 2.0μm because the dependency of I_d upon V_{ds} is exponential. Therefore we forgo the classic model for the exponential term e^{V_{ds}/V_A} in (2). Now that we have supplied empirical verification of our model, let's examine its physical basis.

III. Drain-induced barrier lowering (DIBL)

Fig. 3 shows the cross section of an n-channel MOSFET as well as its energy band diagram (potential versus length along the channel). For a short-channel device, a decrease in the drain's electron potential with respect to the channel (i.e. an increase in V_d) results in a significant drop in the work function between the source and the channel [2]. Since the current density increases exponentially with a decreasing source-to-channel barrier, the channel current is an exponential function of the drain voltage, much as it is in the floating-gate transistor already discussed (Fig. 1). Both processes include barrier lowering at the source due to movement of the drain (although they happen for different reasons). Therefore, we can use (2) to model this phenomena: V_A is a parameter that can be extracted empirically. For long MOSFETs, a large V_A is associated with an exponential curve whose curvature is very small. In fact, the bend in the curve is so small that the slope of $\Delta I/\Delta V_{ds}$ does not change noticeably for the operating range of the device; therefore, the exponential curve appears linear. In summary,

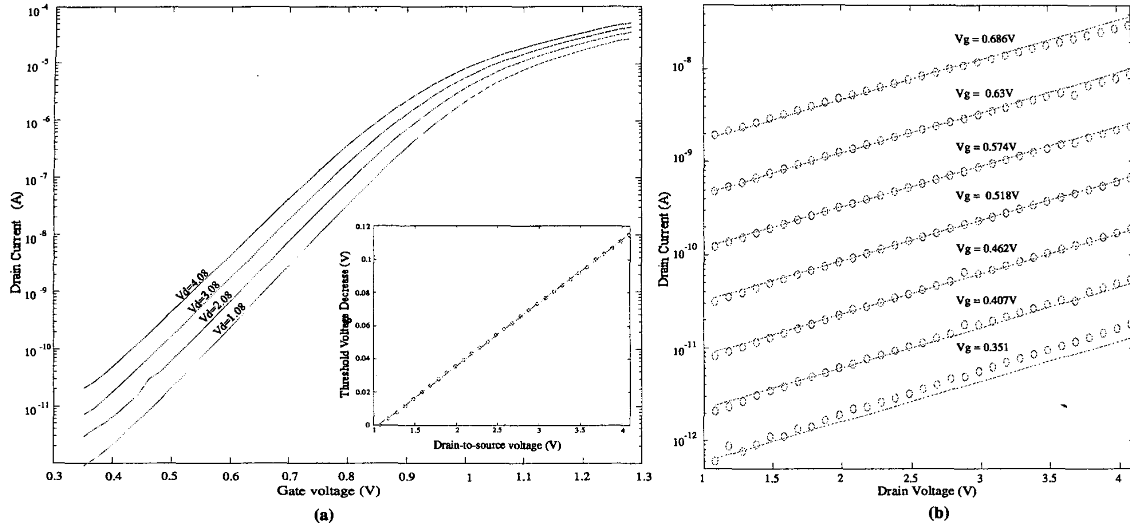

Fig. 4. Measured data from a short-channel MOSFET showing substantial DIBL. (a) Linear curve fit to the threshold voltage shift with drain voltage: slope = 0.0379 V/V (b) Current versus drain voltage for several applied gate voltages. Single curve fit to experimental data: $I = (5.18 \times 10^{-17}) \times e^{0.614V_g/U_T} e^{V_d/1.0V}$

the channel current's dependence on drain voltage looks linear for long-channel MOSFETs, while for MOSFETs with very short channels, the drain current varies exponentially with drain voltage in saturation. Nevertheless, we can use the same expression and a single parameter to model both short-channel circuit effects.

Figure 4b shows empirical evidence of the short-channel MOSFET's exponential dependence of I_d upon V_{ds} over several distinct gate voltages, just as we did for the floating-gate device (Fig. 1). Since both phenomena involve source barrier lowering, we should expect that DIBL also manifests itself in threshold voltage reduction. Figure 4a shows that applying a change in drain voltage noticeably shifts the curve of drain current versus *gate* voltage; in other words, the threshold voltage shifts. The curves are equally spaced for equal changes in drain voltage; hence, the threshold voltage drop is linear. Therefore, we can infer that moving the source barrier is reduced by a linear factor of the drain potential decrease. The inset shows the linear decrease in V_T with an increase in V_{ds}.

Decreasing the channel length results in an increased dependence on drain voltage. Figure 5 shows experimental measurements of Early voltage versus effective channel length for nFETs and pFETs in the same 0.5μm CMOS process. We estimated the effective channel length to be 0.35μm less than the drawn gate length. Both curves show that Early voltage is a linear function of effective channel length; the slope and intercepts of the two curves signifies different device doping profiles.

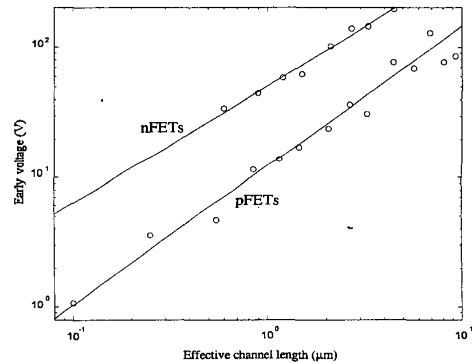

Fig. 5. Measured dependence of Early voltage on effective channel length in a 0.5 μm process for both nFETs and pFETs. The pFET data includes devices at and below the minimum allowed channel length for the processes.

IV. Experimental and Analytical Implications towards Fundamental Amplifiers

We will now show how linear operations in the exponent provide a powerful technique to develop circuits with saturated MOSFETs operating in the subthreshold regime, or BJT circuits biased in the active regime. We can re-

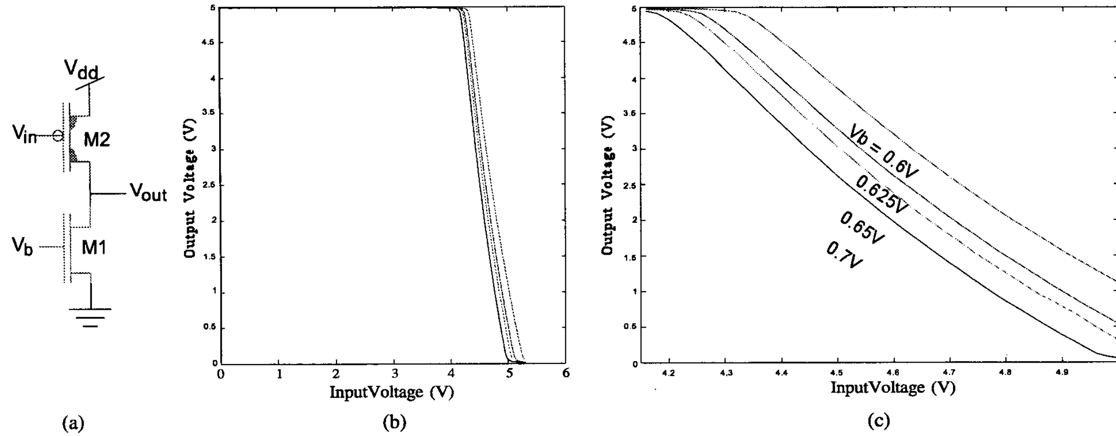

Fig. 6. Amplifier Transfer characteristics with a DIBL pFET device (a) The inverting amplifier with a DIBL pFET as its current source. The DIBL device has a low output resistance (i.e. a low V_A). (b) Voltage transfer function of the amplifier in (a) for various bias currents. Because of the low output resistance, the gain is low; therefore, the input range over which both FETs are saturated is much greater. (c) An enlarged picture of (b). Although the input range is very large (almost a volt), the output function is (approximately) linear over the entire range. The only limitation on this circuit's linearity is device saturation.

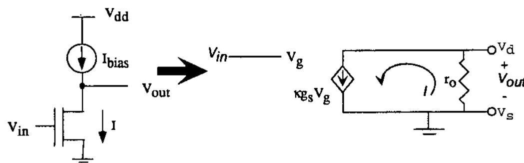

Fig. 7. Circuit and small-signal model of the inverting amplifier with an ideal current source. We may solve for the gain by either using the small-signal model, or merely by using KCL at V_{out} with the large-signal current expressions. The latter option is made simple in subthreshold because of the linear operations in the exponents.

formulate our earlier model, (2), as

$$I = I_o e^{(\kappa V_g - V_s)/U_T} e^{V_d/V_A} = I_o e^{(\kappa V_g - V_s + V_d/A_v)/U_T} \quad (5)$$

where $A_v = V_A/U_T$ is the maximum voltage gain of a subthreshold transistor. If we build a circuit where we fix the channel current, we would predict a linear dependence between V_g, V_d, and V_s, even though we start with a nonlinear equation, throughout the saturation operating region. For example, consider the high-gain amplifier circuit shown in Fig. 6a. The special symbol for the pFET denotes that it is a DIBL device; i.e., it has an ultra-short channel. We use a long-channel nFET current source; therefore its Early effect is negligable. We solve (5) for

$$U_T \ln(\frac{I_{bias}}{I_o}) = \kappa V_{in} + \frac{V_{out}}{A_v}, \quad (6)$$

and therefore the gain from V_{in} to V_{out} is κ V_A / U_T. This gain is a constant for subthreshold currents, similar to the equivalent BJT circuit. Figure 6b and Fig. 6c shows that we get a nearly constant gain over a wide swing of input voltages, as predicted from theory.

One could approach this problem using a small-signal model approach; Figure 7 shows the small-signal model for the circuit in Fig. 6. The model's parameters are obtained by computing the following derivatives of (2): [3]

$$g_m = \frac{\delta I}{\delta V_g} = \frac{\kappa \cdot I}{U_T}, \frac{1}{r_o} = \frac{\delta I}{\delta V_d} = \frac{I}{V_A}. \quad (7)$$

Solving for the amplifier gain, we get

$$V_{out} = -(g_m r_o) V_{in} = -\kappa(\frac{V_A}{U_T}) V_{in}; \quad (8)$$

the gain is identical to the large-signal solution. When a small-signal model is used, all voltage variables are understood to represent small changes in the signal, and therefore this model only predicts this result over a limited range, even though we obtain a similar answer for a large-signal solution over a large-signal range.

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