Basics of Floating-Gate Low-Dropout Voltage Regulators

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Abstract—This paper presents an overview of series voltage regulators, beginning with single-transistor designs and exploring the various design issues and concepts. The regulating characteristics of nFET and pFET single-transistor regulators are compared analytically and experimentally to determine an optimal starting topology. The design of these simple regulators is taken a step further by applying floating-gate techniques to improve the flexibility of the existing design and the ability to customize the regulator bias points.

A voltage regulator converts an input voltage to a fixed output voltage level, and then minimizes any variations in this output voltage caused by fluctuations in the input voltage or the load current. Therefore, voltage regulators are used to supply a stable, ripple-free voltage to integrated circuits to ensure an accurate, low-noise output performance. Series voltage regulators belong to the family of linear regulators where the input voltage is always higher than the output voltage. In these circuits, a regulating transistor is placed in series with the input and output. Since the current through the transistor equals the load current, the output voltage can be regulated by the inherent negative feedback mechanism of the transistor. This mechanism is established by holding the transistor gate or base terminal at a constant voltage. The type of transistor used can be either a bipolar junction transistor (BJT) or a field-effect (FET) device. The following explanation of the feedback mechanism in the series voltage regulator shall be restricted to FETs, although the points presented apply to BJT transistors as well.

In this paper, we present the motivation and present a framework for using floating-gate circuits in voltage regulator design. In Section 1, we describe the basics of regulators by looking at the voltage-regulation properties of a single-transistor element. Before moving into floating-gate regulators, we want to reinvestigate the performance of single-transistors used as voltage regulators; although the performance may not be sufficient for all applications, these techniques might be useful for additional on-chip isolation of small islands between digital and analog blocks. In Section 2, we extend this discussion towards single-transistor floating-gate regulator design. Currently, we are using these results towards building Low-DropOut (LDO) voltage regulators using floating-gate circuits [1]. The results in this paper are based upon experimental measurements in chips fabricated in 2.0μm, 1.2μm, and 0.5μm CMOS processes available through MOSIS.

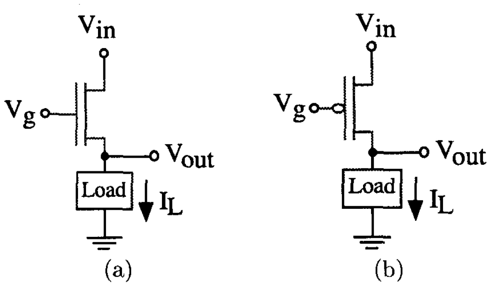

Fig. 1. A series voltage regulator using a (a) nFET pass transistor (b) pFET pass transistor. Notice how the nFET topology is similar to a cascode and how the pFET topology resembles an inverting amplifier. Most commercial Low-Dropout (LDO) regulators are built using pFET pass transistors.

I. Single Transistor Regulators: nFET versus pFET

The nFET series regulator, shown in Fig. 1a, consists of the nFET pass transistor cascoded with its load where the regulator output V_{out} lies in the middle of this cascode. With a fixed gate voltage V_g, V_{out} is protected from variations in both the regulator input V_{in} and the load current I_L. The value of V_{out} is constant for a given I_L and V_g since the transistor will always try to maintain its source voltage below V_g by an offset that depends on I_L. The effectiveness of a transistor as a regulator can be evaluated 2 ways: the V_{out} dependence on I_L for a fixed V_{in} and V_g (*load regulation*), and the V_{out} dependence on V_{in} for a fixed I_L and V_g (*line regulation*). The load regulation can be improved by increasing the ratio g_m / I_L of the pass transistor, because small-signal I_L variations are attenuated at the output by the nFET transconductance (g_m) [1]. We describe the subthreshold nFET or pFET channel current in saturation, I_s, for a change in the FET's floating-gate voltage, ΔV_{fg}, and drain-to-source voltage,

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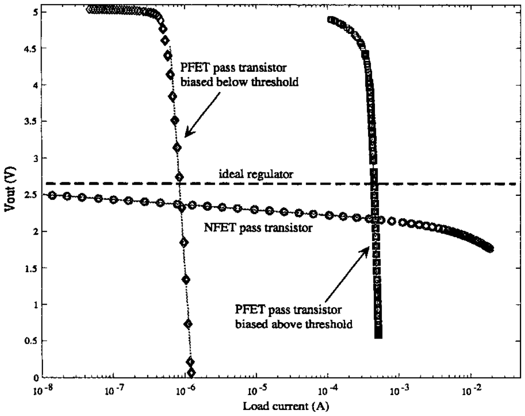


Fig. 2. V_{out} versus I_L measurements for a nFET and pFET single-transistor regulator. For an ideal regulator, V_{out} is independent of I_L. The output of the nFET regulator is much more resistant to load current changes than the pFET version.

ΔV_{ds}, around a bias current, I_{so}, as [4]

$$\begin{array}{ll} \text{nFET:} & I_s = I_{so} \exp\left(\frac{\kappa_n \Delta V_{fg} - \Delta V_s}{U_T}\right) \exp\left(\frac{\Delta V_{ds}}{V_A}\right), \\ \text{pFET:} & I_s = I_{so} \exp\left(\frac{\Delta V_s - \kappa_p \Delta V_{fg}}{U_T}\right) \exp\left(-\frac{\Delta V_{ds}}{V_A}\right), \end{array} \tag{1}$$

where κ_p is the fractional change in the pFET surface potential due to a change in ΔV_{fg}, κ_n is the fractional change in the nFET surface potential due to a change in ΔV_{fg}, V_A is the Early voltage of the nFET or pFET, and U_T is the thermal voltage, $\frac{kT}{q}$. The value of g_m/I_L at subthreshold is different from the g_m above threshold. In the subthreshold region, g_m/I_L is equal to κ/U_T, while g_m/I_L decreases by $\sqrt{I_L}$ when operating the above threshold region; therefore, the best g_m / I_L efficiency is achieved by operating the nFET regulator in subthreshold. The line regulation is dependent on the gain of the regulating transistor; therefore V_{in} variations can be further attenuated by increasing the transistor Early voltage (increasing channel length). Figure 2 shows the experimental dc load regulation measurements made on single-transistor nFET regulator. Ideally, V_{out} should be independent of I_L and the resulting load regulation curve is a horizontal line; the larger the slope of the $V_{out} - I_L$ curve, the poorer the load regulation. The slope extracted from the nFET dc load data in the subthreshold range is 30.8 mV, which is close to the room temperature value of thermal voltage [1]. The nFET regulation performance degrades for above-threshold operation, because this slope then increases in this region.

The topology of a single-transistor pFET regulator, shown in Fig. 1b, is inherently an inverting high gain configuration. Both V_{in} and I_L variations are amplified by a

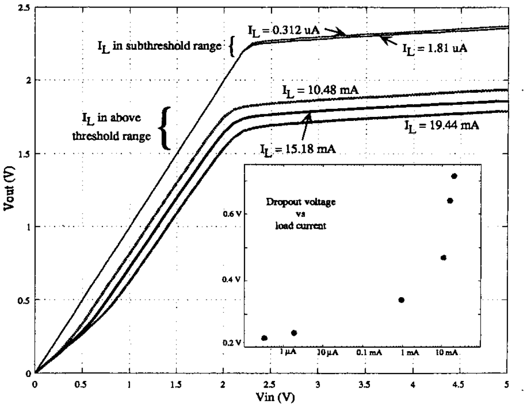


Fig. 3. V_{out} versus V_{in} measurements for the nFET regulator at different load currents. The load for each regulator is an nFET current sink. The dropout voltage corresponding to each load current is shown to increase more rapidly with the load when the nFET pass device operates above threshold. The gate voltage to the nFET regulator was fixed ($V_g = 3$V), while measurements on the pFET regulator were performed for a subthreshold bias ($V_g = 1.1V$ below V_{DD}) and an above threshold bias ($V_g = 2V$ below V_{DD}).

factor of the pFET Early voltage at the output. For load current regulation, the load is connected to the source of the nFET, where the load is connected to the drain of the pFET, resulting in a higher input resistance, and therefore larger voltage variations for given current changes. Figure 2 shows the experimental dc load regulation measurements made on single-transistor pFET regulator. By comparison, the pFET load regulation is much worse since variations in I_L are now amplified by a factor of V_A. Since these properties are undesirable for good output voltage regulation, it can be concluded that the nFET has better load regulation than the pFET device, and is a better pass device in a series regulator. Like the nFET regulator, the load regulation performance of the pFET configuration is shown to be worse when operating above threshold based on the steeper slope of the data in that region.

Figure 3 shows the measured dc line regulation data for the nFET regulator biased with a constant V_g at different values of I_L below and above threshold. The circuit can only regulate when the pass transistor is in saturation; the *dropout voltage* of a FET—the minimum voltage drop across the pass transistor without losing control of the output voltage [2]—is related to its minimum saturation voltage V_{sat}. If the transistor is in subthreshold, V_{sat} is constant (independent of I_L) at the minimum dropout voltage equal to $4U_T$ (approximately 100 mV at room temperature). For a transistor operating above threshold, V_{sat} depends on I_L and the $\frac{W}{L}$ of the device; the larger the transistor, the smaller its dropout voltage. The inner plot in Fig. 3 shows how dropout voltage increases as the

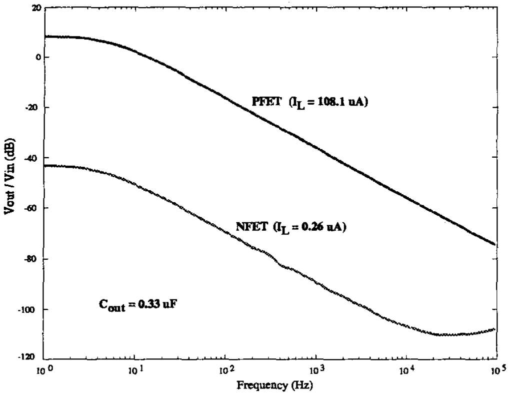


Fig. 4. Measured $\frac{V_{out}}{V_{in}}$ transfer function for a nFET and pFET regulator driving a 0.33 μF load capacitance C_{out}. The pFET regulator load current must be over 400 times larger than the nFET regulator load current to achieve the same dominant pole frequency as the nFET regulator.

load current increases, that is as the transistor goes from subthreshold to above-threshold operation. This performance parameter is particularly significant for integrated circuits in battery-powered electronic devices where the input voltage to the regulator decreases over time. It is desirable to achieve low dropout voltages and maintain regulation even when V_{in} is only a couple hundred millivolts above V_{out} so that the regulators are functional over a wider range of input voltages.

Fig. 4 shows the frequency dependency of V_{out} on small-signal V_{in} variations. Contrary to common lore, both regulators have a single low-frequency pole, where the regulator's rejection improves with increasing frequency. At low frequencies, the magnitude of the transfer function is equal to the dc line regulation [1]. Since V_A is typically much larger than U_T, the output pole of the pFET regulator always occurs at a lower frequency than the pole of the nFET regulator for the same load current. The overall magnitude of the pFET regulator's transfer function is larger than the nFET regulator, because V_{in} variations are amplified at the output by the common-gate configuration of the single-transistor pFET regulator.

Based on the experimental and theoretical analysis of single-transistor regulators, it is concluded that using a nFET pass device in a series regulator structure yields a better regulating performance than a pFET pass device. Furthermore, the regulation characteristics of the nFET regulator can be improved if the pass device operates in the subthreshold region. However, the main disadvantage of using a nFET device is the need to push its gate voltage high enough to turn on the device and drive large load currents while maintaining output voltage regulation. The conventional solution to this problem is to use a charge pump circuit to power the gate-driving circuitry above the power supply rails to achieve the required gate swing. However, charge pump circuits are notoriously noisy and increase the overall complexity of the regulator design.

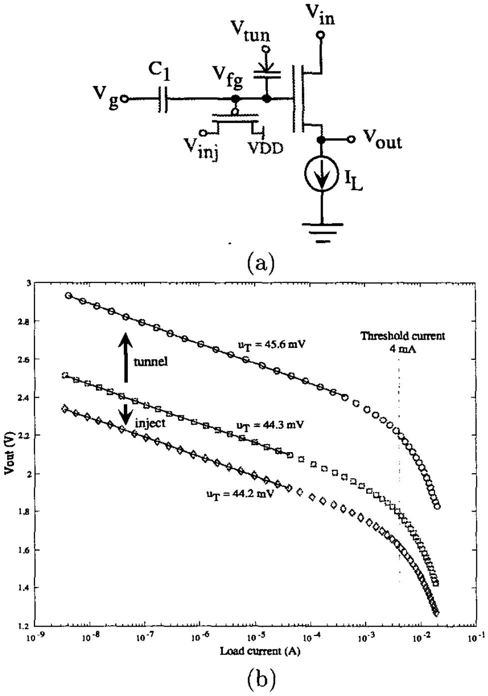
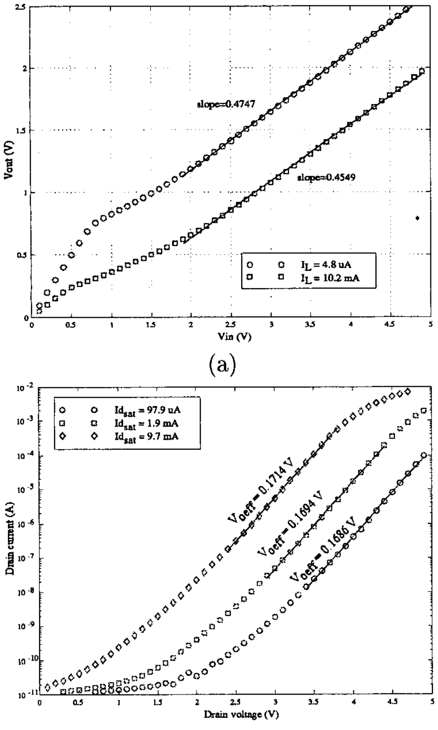


Fig. 5. A single-transistor floating-gate NFET regulator. (a) Circuit diagram. A floating-gate nFET with $\frac{W}{L} \approx 59150$, which is common for pass transistors in conventional series regulator designs; the threshold current was roughly 4.3mA. We show the MOS capacitor used for Fowler-Nordheim tunneling and a pFET used for hot-electron injection. (b) DC load regulation of the floating-gate nFET regulator showing similarity to previous measurements of a single-transistor nFET regulator. The use of a floating-gate pass transistor now allows for V_{out} programmability by tunneling and injection at the floating gate.

II. A SINGLE-TRANSISTOR FLOATING-GATE NFET REGULATOR

If the effective threshold voltage of the nFET is negative, then the charge pump circuitry is not necessary. Using a floating-gate device allows the user to determine the effective threshold of the transistor $I_d - V_g$ characteristic [3], and therefore makes the nFET topology feasible. Making the nFET pass device a floating-gate transistor is a simpler and low-noise alternative to the conventional series nFET regulator design. We change the effective threshold by modifying the charge at the resulting floating



(a)

(b)

Fig. 6. The significant gate-drain overlap capacitance couples drain voltage variations to the floating gate, causing the drain to act like a second gate terminal to the transistor. (a) DC line regulation characteristics of the floating-gate nFET regulator at 2 different load currents. The linearity of this $V_{out} - V_{in}$ relationship is due to the C_{gd} coupling between V_{in} and V_{fg}, which causes the regulator to behave like a source follower for variations in V_{in}. (b) Drain current versus drain voltage characteristics of a floating-gate nFET for 3 different gate biases, showing exponential variation of drain current with drain voltage. Id_{sat} is the drain current for a fixed V_g when $V_d = VDD$.

node; we increase the charge by Fowler-Nordheim tunneling and we decrease the charge by hot-electron injection through a MOSFET.

To verify the feasibility of using a floating-gate nFET pass device in a regulator, it is first used in a single-transistor regulator configuration for comparison with previous measurements. The regulating characteristics of this single-transistor floating-gate regulator should match those of the single nFET regulator, with the additional flexibility of being able to customize the value of V_{out} by changing the amount of floating-gate charge. Figure 5a shows the proposed single floating-gate nFET regulator with the tunneling capacitor and injection pFET connected to the floating-gate for programming. During normal operation, V_{inj} is tied to V_{DD} to cutoff the injection pFET and V_{tun} is tied to a fixed potential, preferably ground to minimize power supply coupling to the floating gate. For the same reasons, the input capacitor C_1 is also grounded. Figure 5b shows the measured dc load regulation of the floating-gate nFET regulator and how the dc value of V_{out} can be modified by tunneling and injection. These curves are similar to the single-transistor nFET load regulation measurements, where the slope in the subthreshold load current range is $-U_T$, and the regulation begins to degrade when the pass transistor enters the above threshold region.

The measured dc line characteristics of the floating-gate regulator are different (Figure 6a) due to the capacitive coupling from V_{in} to the floating gate through C_{gd}. This coupling causes the regulator to behave like a source follower, and V_{out} follows V_{in} linearly. The slope of this $V_{out} - V_{in}$ relationship is smaller than that of an actual source follower with the same-size nFET by a factor equal to the capacitive coupling ratio from the nFET drain terminal to its floating gate. The net capacitive coupling from an applied gate voltage to the channel, κ_{eff} was extracted to be about 0.1, implying that the parasitic capacitances at the floating-gate node are almost as large as or even larger than C_1, causing the capacitive coupling from V_g to the floating gate to be weak. The main source of these parasitics is the overlap capacitance of the large nFET C_{gd} and C_{gs}. Figure 6b shows the measured drain current vs drain voltage curves of the large nFET device alone, which are very similar to its drain current vs gate voltage characteristics. This is because the drain voltage variations couple through C_{gd} to the floating gate, causing the drain terminal to modulate the channel current significantly, as if it were a secondary gate terminal. This floating-gate-to-drain coupling greatly reduces the effective Early voltage of the nFET; we obtained an effective Early voltage of 170mV from measured data.

III. ACKNOWLEDGEMENTS

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