

# A CMOS IMAGER WITH REAL-TIME FRAME DIFFERENCING AND CENTROID COMPUTATION

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## ABSTRACT

We present a novel imager that computes real-time frame difference as well as several image statistics. We desire to use a network of these imagers connected to microprocessors for computation on images. To reduce the bandwidth to the processors, each imager has on-chip computation to determine relevant information and sends only that to the microprocessors. We have developed an imager that uses simple analog elements to implement the desired functions. We present experimental results.

## 1. INTRODUCTION

Biological systems utilize a high level of parallelism in the early stages of visual processing. Many simple elements produce intermediate results simultaneously, and these results serve as the inputs for the more complex, higher brain functions. This computational paradigm reduces the amount of raw data that must be interpreted by the higher stages of the brain. Similar parallel architectures can be leveraged in engineering systems to handle large amounts of data.

One of the main advantages to using many computational elements in parallel is that the individual elements do not have to be powerful to generate useful networks. Rather than concentrating on high image quality, this imager determines simple summary measures of images. Particularly, the imager stores a subtrahend image, and computes the "centroid" of and a "score" for the difference between the transduced and stored images. The *centroid* is the first moment of the absolute value difference image, while the *score* is the global sum of the absolute value difference. Capability for direct scanning is also included, as it is necessary to have direct access to each pixel to store an image.

The imager is fabricated using the AMI 0.5  $\mu\text{m}$  CMOS process. The total die size is  $2.25 \text{ mm}^2$ . As can be seen in Figure 1, the heart of the imager is a  $24 \times 24$  pixel array. Each pixel is  $900 \mu\text{m}^2$  with a fill factor of 18.7%. On the left and upper sides of the array are decoders that provide direct access to each pixel. These are used in direct

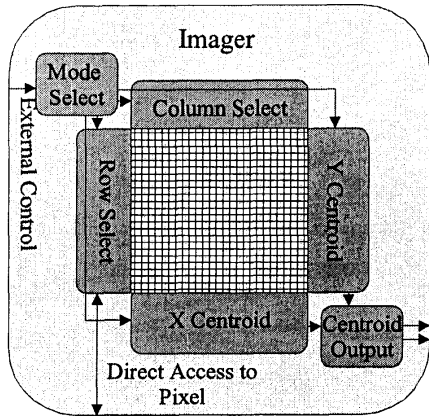
scanning and in memorization of a background image. On the right and bottom of the array is the centroid calculation circuitry. Separate circuitry for each coordinate of the two-dimensional centroid is necessary because the pixels must be connected to common row lines for the  $y$ -centroid and to common column lines for the  $x$ -centroid. Because both circuits share the same pixels, only one coordinate can be calculated at once.

## 2. PIXEL DESIGN

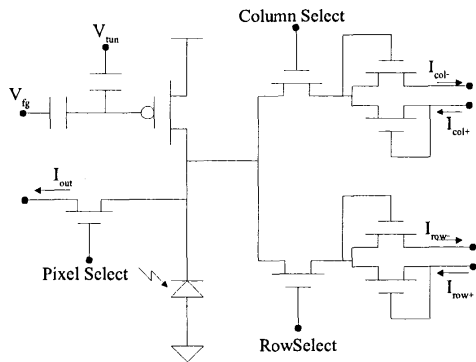
As shown in Figure 2, each pixel consists of a photodiode coupled to a floating-gate  $p\text{FET}$ . The output current from the pixel is the difference between the photodiode current and the drain current of the transistor. Pass transistors, which are controlled by the mode selection logic, steer the output current to one of three different paths: readout, row centroid computation, or column centroid computation. The output for scanning is a bi-directional current, while the centroid outputs from a given pixel are composed of two unidirectional currents, whose directions are fixed by diode-connected transistors. The difference is due to the method in which multiple pixels are connected to the global readout and centroid lines. When scanning, only one pixel in the entire chip is connected to the readout line, but twenty-four pixels—an entire row or column—are connected to a single centroid line. If the centroid lines were bi-directional, the sum current of two pixels could be zero if one pixel were to have a negative current and the next, a positive current. The dual unidirectional line design ensures that the current seen by the centroid circuit is a function of the total change from the background, without requiring full absolute value circuitry within each pixel. It should be noted that both lines must be held at appropriate voltages to prevent current from flowing from the negative line to the positive line through the diode-connected transistors.

The floating-gate  $p\text{FET}$  provides the frame differencing. The transistor's current is a function of the charge stored on the gate. In aggregate, this array of floating gate  $p\text{FET}$ 's provides non-volatile storage for the subtrahend image [1].

### 3. PIXEL OPERATION



**Fig. 1.** Block diagram of the imager. At the center of the chip is a  $24 \times 24$  array of pixels. The circuitry on the lower and right sides of the pixel array calculates the centroid and score. The decoders on the upper and left sides provide direct pixel access for image readout and programming. The control logic in the top left corner receives control signals from external circuitry and provides control signals to the decoders and centroid circuitry.



**Fig. 2.** Pixel Schematic showing a single photodiode, floating-gate transistor, and the current steering circuitry. The output current, which is the difference between the photodiode current and the floating-gate transistor drain current, may be sent to different computational elements by the pass transistors.

The current-steering circuitry in the pixel allows for four different modes of operation: direct readout, programming,  $x$ -centroid computation, and  $y$ -centroid computation. The first mode, direct readout, uses the decoders on the top and left of the chip to connect one pixel to the sense line. The current in the selected pixel is then amplified and digitized by off-chip circuitry. All non-selected pixels are connected to a low-impedance reference voltage. The off-chip amplifier also holds the sense line at the same reference voltage through feedback, reducing transients when switching to the next pixel. Ordered selection of each pixel in the array allows for readout of an image from the chip.

The second mode, programming, also makes use of the decoders. Programming is done according to a process in which each pixel is programmed separately [2]. First, the tunneling capacitor voltage is raised for a duration sufficient to tunnel enough electrons off the floating gates so that all  $p$ FET's in the array are off. The tunneling voltage is then lowered. Then, the injection voltage is raised. The row decoders select one row for readout and hold the drains of the other rows at the injection voltage, insuring that no electrons are injected onto the floating gates of  $p$ FET's in the unselected rows. The gate voltage for the selected column is lowered, enabling injection for the selected transistor. The gates for all other columns are brought high, turning off those transistors. These manipulations insure that only the selected  $p$ FET experiences electron injection on its floating gate. After injection proceeds for a short time, the injection voltage is brought down to the normal power supply level and the current from the pixel is measured. This process is repeated for the selected pixel until the desired programmed current has been achieved. Programming then proceeds to the next pixel in the array.

The remaining two modes,  $x$ -centroid and  $y$ -centroid, are discussed in detail in the next section.

### 4. CENTROID AND SCORE COMPUTATION

Analog circuitry outside of the pixel array is used to compute the centroid and the score of the image. At the end of each pair of row or column lines is the first stage, a current subtraction circuit, as shown in Figure 3. This stage is used in the computation of both measures. The output current is given by:

$$i_{out} = \left| \sum i_+ \right| + \left| \sum i_- \right| = \sum i_+ - \sum i_- \quad (1)$$

In addition to the current mirrors, operational transconductance amplifiers (OTA's) are necessary to hold the current lines at the reference voltage. Computation of the score requires no additional active circuitry. The outputs  $i_{score}$

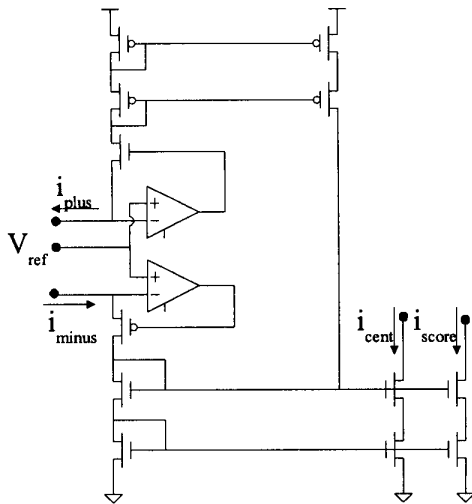


Fig. 3. The absolute summation circuitry. The summation is done using the cascode current mirrors, while the input voltage is set to a fixed value using OTA's.

from each row are simply connected to a common wire to give:

$$i_{score} = \sum_y \left( \sum_x i_+ - \sum_x i_- \right) \quad (2)$$

which is the sum over the entire array of the difference between the current image and the stored background.

For computing the  $x$ -centroid, the pixels are connected to common positive and negative current lines for each column; for the  $y$ -centroid, for each row. The currents in each line then give current for the sum of the positive current and the sum of the negative current.

The centroid is computed by using an aggregation network of differential pairs [3]. The voltage inputs ( $V_n$ ) to the amplifiers vary linearly between  $V_{max}$  and  $V_{min}$  with position [4]. The bias currents for each amplifier are the absolute value sum currents from each column, or from each row, depending on the operating mode. Each differential pair remains in its linear range so long as

$$V_{max} - V_{min} < 4 \frac{kT}{q} \quad (3)$$

remains valid. Assuming linearity in each pair, the output

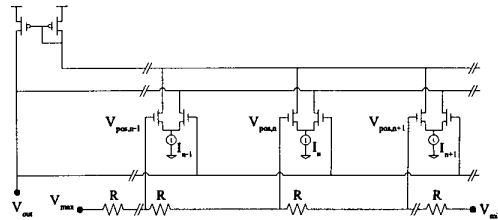


Fig. 4. One dimensional centroid network which produces an output voltage equal to the position voltage of the centroid. It is a modified aggregation network. The resistive divider provides the position encoding.

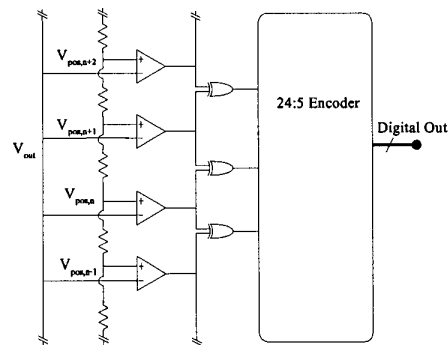


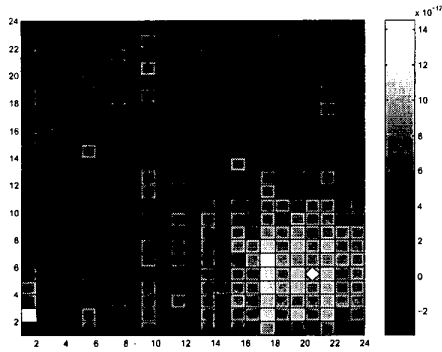
Fig. 5. The flash analog to digital converter in the centroid array. The input to the ADC is the  $V_{out}$  from the analog network. The comparators are OTA's operating without feedback. The output from the ADC is a 5-bit digital word representing the location of the centroid.

voltage is given by:

$$V_{cent} = \frac{\sum i_n v_n}{\sum i_n} \quad (4)$$

If the voltage difference across the centroid network exceeds 100 mV, some of the differential pairs become saturated and the output voltage approximates a median position rather than the mean as indicated in (4).

The second stage in each centroid element compares the centroid voltage to the position voltage ( $V_n$ ) in order to generate a digital representation of the centroid. For  $0 \leq n \leq N$ ,  $V_n$  is compared to  $V_{centroid}$ , and the circuit creates a binary-valued vector that consists of some number of 1's followed by 0's. That vector is then transformed using an array of XOR's into a one-hot vector which consists of all



**Fig. 6.** Result from direct readout of the imager. The scale on right is in amperes. The imager is focused on an LED, which is in the lower right of the visual field. The centroid position, shown as a white diamond, correctly tracks the location of the LED.

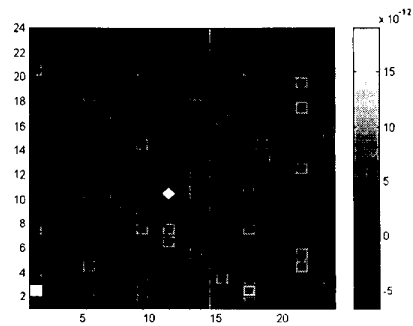
0's except for a single 1. The position of that 1 indicates the row (column) at which the centroid exists this address is then encoded into a digital word.

## 5. EXPERIMENTAL RESULTS

The imager has been tested in direct readout and in centroid mode. For current readout, an off-chip switched-capacitor transimpedance amplifier converts the current into an analog voltage. The analog voltage signal is then sampled using the ADC of a microcontroller. Double sampling is used to reduce noise and offsets [5]. The digital centroid data could be read directly by the microcontroller's digital I/O lines. An entire frame could be read in 1.5 s.

An image, shown in Figure 6, was taken with the imager focused on an LED. The total score was 1.75 nA. The LED was purposely positioned in the bottom right of the visual field to provide a non-trivial demonstration of the centroid output. The bright pixel at row 1, column 2 seemed to be an artifact of the measurement setup. An alternative method of computing the score was to take the absolute value sum of the measured currents with a numerical software package; this method yielded a score of 1.27 nA. This shows reasonable agreement with the directly measured value.

Another image, shown in Figure 7, was taken with the imager covered, giving the dark current. The score for the dark current was 17.2 pA. As the pixel currents were relatively uniform across the entire array, the centroid position was near the center of the array. Using numerical software to compute the score gave 1.00 nA. As this was much greater than the score measured directly, it is likely that most of the measured currents were actually noise introduced by the off-chip amplifiers. This gave a noise floor for reliable measurements on the order of 5 pA. It is likely that this noise



**Fig. 7.** Result from direct readout of the imager. The scale on right is in amperes. The imager is covered, so that there is no incident light onto the photodiodes. The centroid position, shown as a white diamond, is near the center of the array.

floor is a function of the test setup used in the experiment, and not a limitation of the chip itself.

## 6. CONCLUSIONS

We have developed a CMOS imager with centroid computation and non-volatile storage for frame differencing. The imager has application as a smart sensors in low power and distributed image analysis systems. Experimental results of image and centroid readout have been presented.

## 7. REFERENCES

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