

# LOW-POWER ANALOG IMAGE PROCESSING USING TRANSFORM IMAGERS

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## ABSTRACT

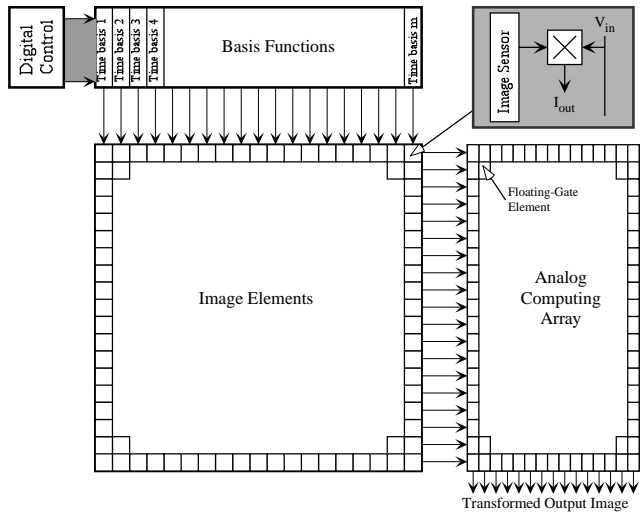
We introduce our Transform Imager Technology and Architecture. This approach allows for Retina and higher-level bio-inspired computation in a programmable architecture that still possesses similar high-fill factor pixels of APS imagers. This imager is capable of programmable matrix operations on the image, where we can represent the image as either a full matrix or using block matrix operations. The resulting data-flow architecture directly allows computation of spatial transforms, motion computations, and stereo computations. The core imager performs computation at the pixel plane, but still holds to a fill factor greater than 40 percent. Each pixel is composed of a photodiode sensor element and a multiplier.

We introduce our Transform Imager Technology and Architecture. This approach allows for Retina and higher-level bio-inspired computation in a programmable architecture that still possesses similar high-fill factor pixels of CMOS imagers. Figure 1 shows the block diagram of our Transform imagers. If the incoming voltages represent functions in time, particularly transform bases like sine and cosine, then we are performing computations analogous to matrix image transforms. The output is a continuous stream of each row of the transformed image, repeated over a desired fundamental frequency. This approach is enabled by floating-gate circuits [2], in storing arbitrary analog waveforms for image transforms, in programming waveforms to account for average device mismatch, and in computing additional matrix-vector computations.

We present our approach in the following sections. In Section 1, we describe our transform imager concepts. This imager is capable of programmable matrix operations on the image, where we can represent the image as either a full matrix or using block matrix operations. In Section 2, we present the resulting data-flow architecture for image processing built around this transform imager. In Section 3, we discuss some circuit specific issues to the overall signal processing of the basic Transform imager.

## 1. TRANSFORM IMAGER COMPUTATION

Our transform imager cell performs computation at the pixel plane, but still holds to a fill factor greater than 40%, and allows for retina and advanced biological-type processing. Therefore, we have the best of both worlds in a single architecture. This imager is capable of programmable matrix operations on the image, where we can represent the image



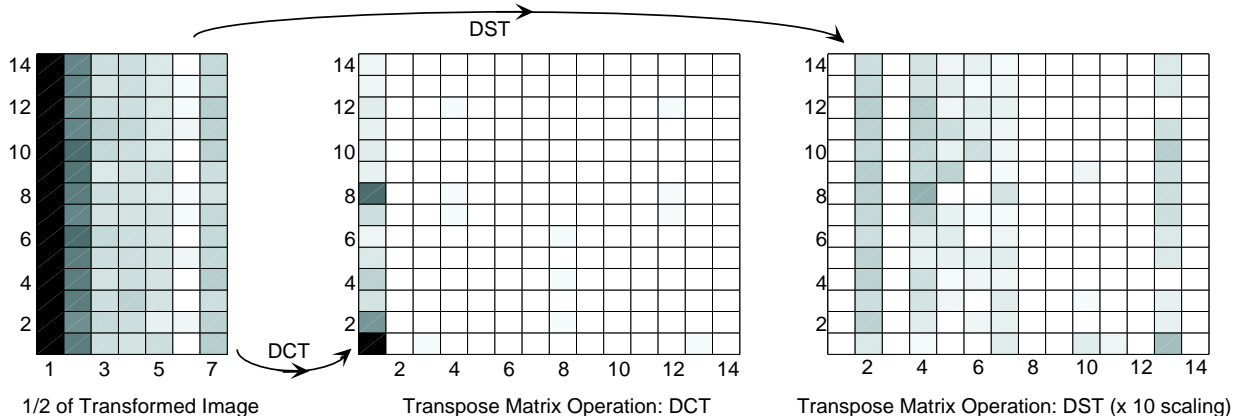
**Fig. 1.** Top view of our matrix transform imager. The image output rate will be the same as the time to scan a given image; then the resulting image transfer rate is significantly reduced if information is refined. Approach allows arbitrary separable matrix image transforms; these transforms are programmable because we use floating-gate circuits. Voltage inputs from various time bases are broadcast along columns, and output currents are summed along lines on each row. Each pixel processor multiplies the incoming input with the measured image sensor result, and outputs a current of this result. Time basis could be oscillators, pattern generating circuits, or arrays or stored analog values (i.e. floating-gate storage). With can compute block image transforms with smaller time bases, digital control, and smaller block matrices for block image transforms. Finally, we can get multiple parallel results, since all of the matrix transforms could operate on the same image flow.

as either a full matrix or using block matrix operations. The pixel for the Transform imager has a fill factor greater than 40%, which allows for retina and advanced biological-type processing, in a programable architecture that still preserves the overall high fill-factor of APS imager for the pixels.

This Transform imager can compute arbitrary separable matrix transforms. We perform separable matrix transforms as

$$\mathbf{Y} = \mathbf{A}^T \mathbf{P} \mathbf{B} \quad (1)$$

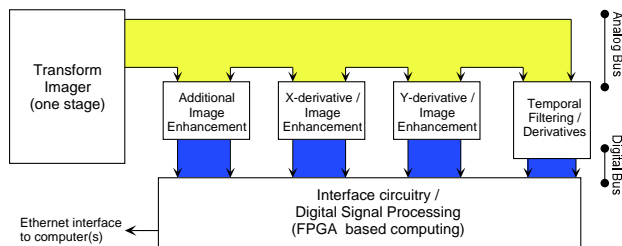
where  $\mathbf{P}$  is the row and column array of pixels,  $\mathbf{Y}$  is the computed output image array,  $\mathbf{A}$  is a transform matrix corresponding to the transform on the image plane by the basis functions, and  $\mathbf{B}$  is a transform matrix corresponding to the floating-gate enabled transform after the image plane. The values of  $\mathbf{A}$  are stored in an analog floating-gate array typically on the imager IC, and applied to the pixel column



**Fig. 2.** Experimental data from a 14 x 14 test imager. We present one half of the output image after transforming the image (uniform illumination) using sine waves. The output image is symmetric; therefore we have output only the first half. **DCT Transform:** Result of an additional Cosine transform on initial sine-transformed imager data. We nearly get the ideal impulse function at (0,0) position, as predicted by taking a 2D Cosine transform of an image of uniform illumination. **DST Transform:** Result of an additional Sine transform on initial sine-transformed imager data. The plot of this Sine transform multiplied by a factor of 10 in comparison with the Cosine transform; without the scaling factor (x 10), the image would look nearly white. We get nearly zero matrix as we would expect for an input image of uniform illumination.

inputs. Further, if the input waveforms are continuous, then the result is a continuous waveform, resulting in added computational options. For example, the choice of output signal sampling will result in different discrete-time inspired computations with an identical setup. For this paper we will concentrate on computing DST / DCT like transforms of the image as a representative of possible matrix computations. To characterize this imager, we will compute these transforms for uniform illumination; the ideal DST would be all zeros, and the ideal DCT would be an impulse at position (1,1).

We present experimental data from a small  $14 \times 14$  image block, requiring roughly  $150 \mu\text{m} \times 200 \mu\text{m}$  for the array in  $0.5 \mu\text{m}$ . We will discuss the overall computation using a  $14 \times 14$  pixel array in the context of DST and DCT transforms. Figure 2 shows the results of DST/DCT type transforms on a uniformly illuminated image. We input sine waves of integer frequencies and obtained the first image result by sampling at  $\pi/2$  phase of the primary harmonic (this transform is symmetric, so we show only the first half of the output waveform). From the resulting waveforms (not sampled waveforms), we computed the second matrix transform using DST coefficients and then for DCT coefficients. We see some distortion in the transformed images, which correlates well to harmonic distortion from the differential pairs. Since the input patterns are fixed, the effect of harmonic distortion is fixed and appears as additional spatial (smoothing) filter. In practice we can account for this additional linear spatial filter, by modifying the matrix transform coefficients to account for this filter. In the same process, we have scaled this imager to a functional  $128 \times 128$  imager with matrix processing for  $16 \times 16$  block transforms in an area of  $4 \text{mm}^2$ . The results can be extended to arbitrary matrix transforms.

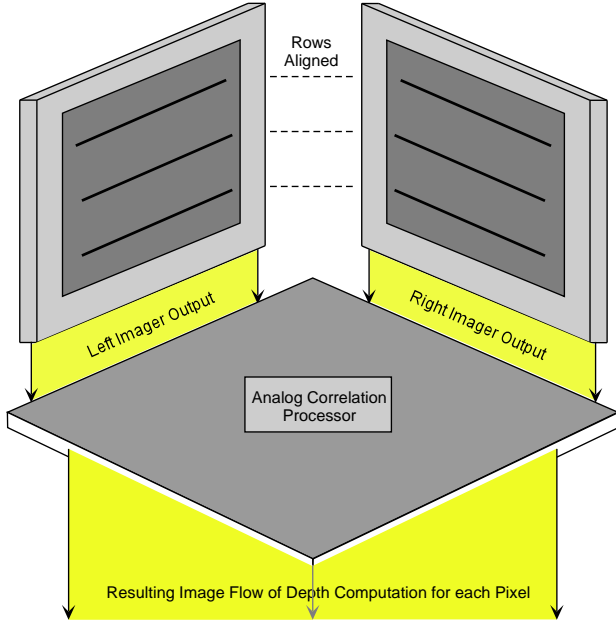


**Fig. 3.** Block diagram of a motion (optical-flow) computation system. This system computes the two spatial derivatives (x and y), a temporal derivative, and a filtered version of the original image. Computing gradients in x, y, and time are necessary for optical flow computation; we can make fairly smooth derivative operations in the spatial coordinates by combining a smoothing filter with the derivative kernel over a moderate window size ( $16 \times 16$  or greater). The time derivative is computed by subtracting two (or more) successive frames, which requires a sample and hold for each image frame.

## 2. IMAGE PROCESSING ARCHITECTURE BASED ON THE TRANSFORM IMAGER

The transform imager architecture is both modular and programmable making it ideal for image data-flow computations. This architecture's scalability makes it feasible to compute large-scale, digital-camera resolution images. Furthermore, the image processing architecture computes on the image plane allowing for data reduction that is compatible with machine vision and biological modeling. The sensor can be used to subsample the incoming data if desired, or if the resulting system can handle the data rate, can be passed on so that easier refinement could occur further up the processing chain, either by additional analog circuitry, or additional digital processing.

This architecture is modular because the output data flow is a sequence of columns from an image; this image is either from a set of sensors or the output of some amount of



**Fig. 4.** Picture using two transform imagers to compute stereo computation. Because each row is aligned with another row on the second imager along the same axis, finding depth for each pixel is a row by row operation, which maps directly into the transform imager's output. The inputs to the stereo processing could be outputs from two imagers, or any symmetric processing starting from two imagers. The resulting computation is similar to Maholwald's one-dimensional stereo imager design [18], although a variety of algorithms can be computed using this architecture.

signal processing. We can have multiple image processing steps, where each intermediate result can be acquired by the controlling digital system for higher levels of processing. Further, the outputs are continuous waveforms, allowing for time-domain filters to be used to obtain spatial responses and image interpolation.

In the following subsections, we will address several key features of this architecture, as well as design issues associated with this architecture. We will describe some basic transforms, and interfacing issues in the following three subsections. In the last two subsections, we will apply these concepts to two practical case studies.

### 2.1. Additional Matrix Image Transforms

Because the data flows through each processor a column or row at a time, we can perform matrix operations (by image matrix) on an image by a sequence of matrix-vector computations on the image flow. We can perform matrix-vector computations using our existing Analog Computing Array (ACA) technology based upon floating-gate circuits [1], which is related to dense implementations of neural networks. Further, any of these matrix transforms also transposes the image; therefore, in two matrix-vector operations, we can compute any separable matrix transforms. For example, we could perform 2D DCTs, image smoothing, edge enhancement, and differentiation. In particular, one could

compute *clean* derivatives by incorporating smoothing into a derivative kernel. Finally, we can get multiple parallel results, since all of the matrix transforms could operate on the same image flow. One could envision using this approach for real-time image compression based upon DCT transforms and/or vector quantization,

### 2.2. Temporal filtering

One interesting question with this flow model is how to perform temporal filtering. We could either build the filters directly into the pixel, which would result in much larger pixels and greatly increase the system cost for a given resolution, or we could store a delayed version of the transformed image. This approach requires a temporary storage array for currents or voltages for each delay; therefore one would be practically limited by the number of delays in building temporal filters. Our approach is to build a set of current sample-and-hold elements into an array that could be used for temporal filters; one can build dynamic current sources that can store their current at reasonable accuracy for seconds, particularly with on-chip compensation of leakage through MOSFET switches. Temporal filters should be used sparingly, or after spatial compression, due to the number of required sample-and-hold elements. Also, continuous time filters (i.e differentiators) perform spatial filtering. These filters will have less flexibility than the matrix transforms but also have much smaller space requirements.

### 2.3. Interfacing between blocks

In practice, one must also consider the interface between computation blocks. For a 1024 x 1024 imager computing at a 60Hz image rate requires a parallel data rate (1024 signals) of 120kHz. If two blocks are adjacent on the same IC, then this data rate is trivial to accommodate. If these signals are being passed between chips, requires over 100M analog samples per second, which is a more challenging specification. This rate is similar to simply reading out pixels from any standard CMOS array. Each pixel could be directly read out in a transform imager, since a column scan is equivalent to multiplication by a digital value moving by one position for each step. In general, this issue is significant when interfacing to a digital system, since multiple "images" could be transmitted to the controlling digital system.

### 2.4. Case I: Preprocessing for Optical Flow

Figure 3 shows the block diagram using these imagers and additional matrix computations as a front-end processor to compute optical flow. One must compute separate spatial (for x and y directions) and temporal differencing blocks. The spatial differencing blocks are either matrix transforms with a derivative kernel, or continuous-time derivative circuits. The temporal differencing block requires a set of current sample-and-hold elements are built into an array that

could be used for computing temporal derivatives of this image. One could imagine using these outputs that compute optical flow that could be used by digital processing to compute global displacement estimation, target tracking, and time-to-contact computations,

## 2.5. Case II: Depth from Stereo

Figure 4 shows a block diagram using these transform imagers to compute depth from two imagers (Stereo image processing). Since the two imagers have pixels aligned along one axis, computing depth from stereo only requires computing depth from a row by row basis. In our architecture, a row by row basis is instantaneously computing this function based upon successive outputs from the two transform imagers. The resulting computation is similar to Maholwald's one-dimensional stereo imager design [18], although a variety of algorithms can be computed using this architecture. Further, one could also imagine similar algorithms to compute three-dimensional motion enabled by two or multiple imagers.

## 3. CIRCUIT DISCUSSIONS ON THE TRANSFORM IMAGER

In this section, we discuss some circuit specific issues to the overall signal processing of the basic Transform imager built in a standard CMOS process. We will discuss the basic processor structure of the computation (multiplication) of the sensor signal in each Pixel. This approach could include more advanced image sensors elements/circuits with a corresponding modification to the resulting fill factor. We will present results from a signal pixel, the resulting computation, and effect of mismatch and offsets through this circuit. We also briefly describe the similarities of this transform imager to other photodiode based imagers.

### 3.1. Transform Imagers as a Mixture of CMOS Imagers and Retinas

Imagers based on photodiodes tend to be characterized as either bioinspired, such as retina models or other focal-plane processing, or as closer to APS image sensors. Transform imagers borrow both from focal-plane imagers like retinas as well as standard CMOS and random-access imagers to create this unique architecture.

The first widespread research in silicon imagers that enabled further computations started with the silicon Retina, a biologically inspired neural systems that originated from Carver Mead's group [3, 4, 7]. These processors modeled the edge enhancement properties in the early retina processing based upon photodiodes and phototransistors that naturally occur in a silicon CMOS process. Future designs improved so to be usable in systems at high density levels [6, 7, 8] and for high performance [5]. Typically, because of the large pixel size and research costs, these cir-

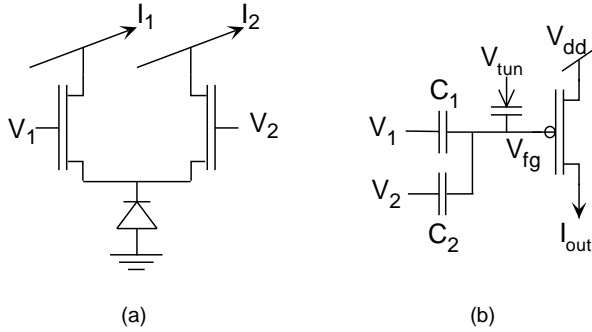
cuits are rarely built for large image processing, but are typically focused at machine vision tasks where the required pixel count is one to two orders of magnitude less. From these retina chips, several higher level processing ICs have been built to investigate stereo processing [17, 18], communication architectures for action potentials [9], attention computations, and motion [10, 11, 12, 13, 14, 15, 16]. Typically, because of the large pixel size and research costs, these circuits rarely compute on large images, but are typically focused at machine vision tasks where the required pixel count is one to two orders of magnitude less.

CMOS imagers took a related route to the silicon retina models. These approaches, typically credited as started by Fossum, et. al, [19, 20, 21, 22, 23, 24, 25, 26, 27] worked with photodiode based arrays with minimal circuitry in the pixel, resulting in large imaging arrays, and therefore a technology viable for digital cameras and is a platform for more sophisticated computations. To characterize the spatial efficiency of a pixel, the concept of fill-factor, which equals the ratio of image sensor area over the pixel area, is defined; the larger the fill-factor, the larger the resulting imager that can be built. Typical CMOS imagers have fill factors from 50% to 30%; typical focal plane imagers have fill factors around 1% to 4%.

Our transform imager cell performs computation at the pixel plane, but still holds to a fill factor greater than 40% like APS imagers, and allows for retina and advanced biological-type processing. Therefore, we have the best of both worlds in a single architecture. This imager is capable of programmable matrix operations on the image, where we can represent the image as either a full matrix or using block matrix operations.

### 3.2. Basic Pixel Element

Each Pixel is composed of a photodiode sensor element and an analog multiplier. Figure 5a shows that the circuit element for this multiplication is an nFET differential pair. For the differential pair operating with subthreshold bias currents (which should always be the case due to the low-level image sensor currents), we can express the differential output current when the circuit is in its linear range as the product of the sensor current and the applied differential voltage. Each pixel could be directly read out by this technique, since a column scan is equivalent to multiplication by a digital value moving by one position for each step ( $\tanh(x) \approx 1$  or  $-1$  for large  $x$  magnitudes). A single pixel could include more advanced image sensors elements / circuits with a corresponding modification to the resulting fill factor. Offsets in differential pairs are important for most analog design problems, and is no exception for this imager. We present elsewhere that this imager concept is insensitive to offsets in the differential pair if the signal swing is held in the device's linear range, even for small transistor sizes [2].



**Fig. 5.** Key circuit elements for the Transform imager technology. (a) **Pixel element:** To multiply the transduced photodiode current by incoming basis functions, we use a differential pair to modulate a fraction of the sensor current through the transistors. For sufficiently small differential input voltages, we get a linear multiplication, as illustrated in the resulting experimental data. The simplicity of the pixel circuit results in fill factors competitive with APS imagers. (b) **Floating-gate transistor:** This circuit can store a current based upon the charge at the floating-gate node. Therefore we use this element to store the basis functions for the Transform imagers. This circuit can also be used as a transistor, and when operating with subthreshold currents, this transistor computes a product of the input voltage with the stored current. Therefore, we use this element in the matrix-vector multiplication memory arrays.

In applications where very high performance (and therefore nearly zero offsets) is required, one could use floating-gate tuning techniques for differential pairs [27], with the accompanying decreases in fill factor. Our measurements show that a single pixel element shows little change from dc to 100Hz for typical fluorescent lights. This frequency response will be dependent upon the incoming light levels; we finally see a corner frequency at 30Hz for 4 orders of magnitude lower light intensity from average room light. From these measurements, we expect sufficient bandwidth for a 1024 x 1024 imager performing full matrix operations at 60Hz image rate.

### 3.3. Imager Technology enabled by Floating-Gate Circuits

This approach is enabled by floating-gate circuits in three ways. First, we can store arbitrary analog waveforms enabling arbitrary matrix image transforms or block image transforms. Second, we can program these waveforms to account for average device mismatch along a column, thereby getting significantly higher image transform quality. Third, we can use floating-gate circuits to compute additional matrix-vector computations. A floating-gate matrix-vector computation block is also known as an Analog Computing Array (ACA) [1]. This system using the output image stream will compute a transposed matrix transform; therefore we can directly compute arbitrary separable matrix transforms. Some examples of this processing include image filtering, computing spatial derivatives, and 2D spatial transforms, like 2D DCT and 2D DST. In particular, one could compute *clean* derivatives by incorporating smoothing into a derivative kernel.

## 4. CONCLUSION

We introduced our Transform Imager Technology and Architecture. This approach allows for Retina and higher-level bio-inspired computation in a programmable architecture that still possesses similar high-fill factor pixels of APS imagers. This imager is capable of programmable matrix operations on the image, where we can represent the image as either a full matrix or using block matrix operations. The core imager performs computation at the pixel plane, but still holds to a fill factor greater than 40 percent. Each pixel is composed of a photodiode sensor element and a multiplier. Further, the resulting data-flow architecture directly allows computation of spatial transforms, motion computations, and stereo computations, in a straightforward on-chip or multi-chip architecture.

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