

17.3 A 2.5V 14-bit $\Sigma\Delta$ CMOS-SOI Capacitive Accelerometer

Babak Vakili Amini, Siavash Pourkamali, Farrokh Ayazi

Georgia Institute of Technology, Atlanta, GA

Low cost high precision MEMS accelerometers with near μg resolution and stability are needed in a number of applications ranging from GPS-augmented inertial navigation systems to guidance and stabilization of satellites and spacecrafts [1]. This paper presents a truly 14b $\Sigma\Delta$ modulator interface IC for a high-resolution SOI capacitive accelerometer fabricated in a simple stictionless process that improves the performance and manufacturability of high-sensitivity accelerometers. The interface IC is designed and fabricated in the 2.5V 0.25 μm 2P5M N-well CMOS process provided by National Semiconductor and interfaced with the accelerometer chip using wire-bonds. Power consumption is 6mW including an on-chip multiphase clock generator for data sampling. The measured resolution of the accelerometer system is 110 μg at 75Hz with a 1Hz resolution bandwidth (RBW) and dynamic range of 85dB. The resolution is limited by the sensitivity of the accelerometer.

The accelerometers were fabricated on 40 μm thick low-resistivity (<0.01 $\Omega\cdot\text{cm}$) SOI wafers using a simple, backside dry release, low temperature process comprising of two masks and only three plasma-etching steps. The fabrication process flow and the SEM of a prototype device are shown in Fig. 17.3.1. The buried oxide of the SOI substrate provides electrical isolation between the electrodes.

Figure 17.3.2 shows the architecture of the implemented fully differential input/output $\Sigma\Delta$ interface IC. In contrast to previously reported accelerometer $\Sigma\Delta$ interface architectures in which the MEMS accelerometer was directly connected to the first stage integrator of a $\Sigma\Delta$ modulator [2-5], this architecture relies on a front-end block which consists of a fully differential input/output switched-capacitor charge amplifier followed by a sample and hold stage. The back-end block consists of an anti-aliasing filter and a first-order $\Sigma\Delta$ modulator, comprised of a fully differential input/output integrator, a clocked comparator and negative feedback network. The sample and hold at the output of the front-end block provides a smooth signal that is band-limited by the anti-aliasing filter. To reduce flicker noise and offset, two stages of a correlated-double-sampling (CDS) scheme is used in the charge amplifier and in the $\Sigma\Delta$ integrator, and optimized dimensions for the input transistors are devised. As shown in Fig. 17.3.3, the double-stage CDS technique is able to uniformly reduce the flicker noise of the interface IC by 10dB (measured by comparing implementations with and without CDS) without the need for chopper stabilization. The front-end charge amplifier not only reduces the noise contribution of the preceding $\Sigma\Delta$ to the overall noise floor of the IC (due to programmable high gain of the charge amplifier), but also adds the ability of interfacing the IC with different accelerometers without compromising the optimized operation of the $\Sigma\Delta$ modulator. Also the use of CDS in the back-end integrator provides the flexibility to reduce the gain of the front-end block without compromising the noise performance of the system when the charge amplifier is configured as a buffer. The front-end and back-end blocks each have a dynamic range of 85dB or larger. Long CMOS switches are used to reduce clock feedthrough and appropriate delayed clocks with their complements are provided to reduce charge injection of switches.

A folded-cascode architecture is chosen for the fully differential operational-transconductance amplifier (OTA) in the switched capacitor amplifier and integrator. Figure 17.3.4 shows the transistor-level schematic of the implemented OTA including contin-

uous-time common-mode feedback circuit. The OTA is self-compensated via the load capacitance. The input stage utilizes large PMOS transistors (M1, M2) to reduce flicker noise. The transconductance (g_m) of the input transistors are designed to be large enough to avoid noise contribution of other transistors. Also the lengths of the load transistors (M4, M5) is larger than the length of the input transistors. The biasing voltages Vb1, Vb2 and Vb3 are generated from a bootstrapped current reference derived from a band-gap voltage reference. The measured temperature coefficient (TC) of the band-gap is 40ppm/ $^{\circ}\text{C}$. A continuous-time differential averaging amplifier (DAA) configuration is used for the common-mode feedback circuit.

A voltage-controlled relaxation oscillator is designed to generate the on-chip sampling clock and required phases. The schematic of the relaxation oscillator is shown in Fig. 17.3.4. The duty cycle and the frequency of the oscillator are adjustable independently using the control voltages $V_{\text{ctrl},2}$. The two levels of the fast voltage-level detector are defined as 0.25 V_{dd} and 0.75 V_{dd} , which control the charge and discharge of the oscillator's capacitance. The sampling clock frequency is 1MHz with a 50% duty cycle.

The anti-aliasing filter that precedes the sample and hold stage is a buffered MOSFET-C low pass filter with a -3dB frequency of 50kHz. The MOSFETs are biased in ohmic region and do not generate significant flicker noise. However the thermal noise generated by these MOS resistances is added to the input signal of the $\Sigma\Delta$ modulator and act as a dithering mechanism to randomize the quantization noise spectrum. Figure 17.3.5 shows the output noise spectrum of the interface IC, illustrating the noise shaping effect of the modulator and the up-conversion of the quantization noise. The interface IC achieves a dynamic range of 85dB at 75Hz, which is equivalent to a resolution of 14b (capacitive resolution of 22aF). Figure 17.3.6 shows the summary of the measured specifications of the sensor and the interface IC chips. The measured differential static response of the accelerometer and the front-end charge amplifier to external acceleration is shown in Fig. 17.3.7, corresponding to a sensitivity of 500mV/g. The active die area of the interface IC is 2mm².

Acknowledgements:

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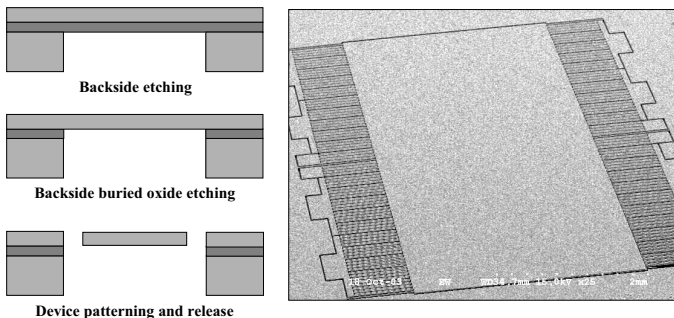


Figure 17.3.1: The dry-released SOI accelerometer fabrication process and SEM.

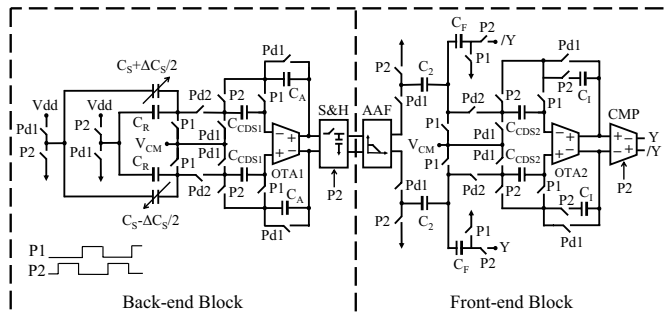


Figure 17.3.2: Architecture of the implemented Sigma-Delta interface IC.

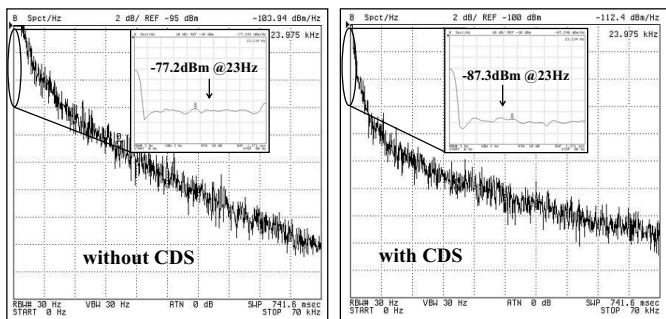


Figure 17.3.3: A comparison of the output flicker noise for implementations with and without CDS.

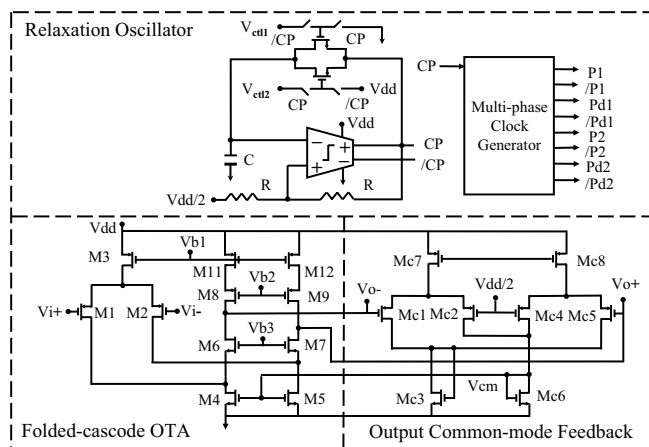


Figure 17.3.4: Transistor level schematic of the implemented OTA and on-chip clock generator.

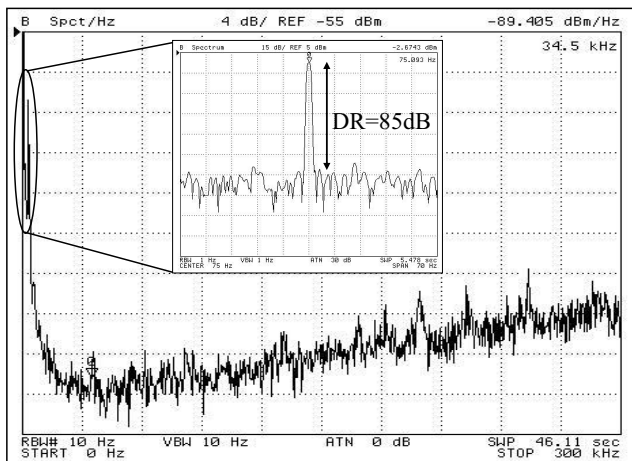


Figure 17.3.5: Measured up-converted quantization noise spectrum.

Sensor Specifications	
Device size	4mm×3.5mm×40μm
Rest capacitance	5.3pF
Sensitivity	0.2pF/g
Brownian Noise floor	1μg/rtHz
IC Specifications	
Sampling Clock	1MHz
Dynamic Range	85dB (equivalent to 14-bit)
Sensitivity	0.5V/g
Full scale	±2g
Minimum Detectable Acceleration	110μg @ 75Hz (RBW=1Hz) 16μg @ 10kHz (RBW=1Hz)
Capacitance Resolution	22aF @ 75Hz (RBW=1Hz) 4aF @ 10kHz (RBW=1Hz)
Power Dissipation	6mW
IC Die size	2mm ²

Figure 17.3.6: Measured specification summary of the sensor and interface IC.

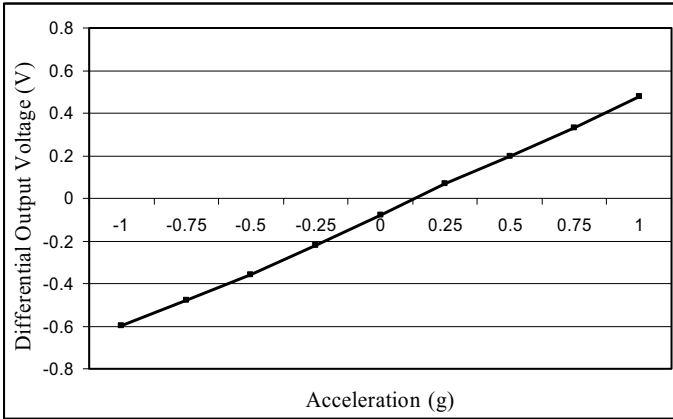


Figure 17.3.7: Static differential-output response to the accelerations in $\pm g$ range.