

A 7-MHz Process, Temperature and Supply Compensated Clock Oscillator in 0.25 μ m CMOS

Krishnakumar Sundaresan, Keith C. Brouse*, Kongpop U-Yen, Farrokh Ayazi and Phillip E. Allen

School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA 30332-0250
Email: ayazi@ece.gatech.edu; Tel: (404) 894-9496; Fax: (404) 894-4700

*now with Texas Instruments Inc., Dallas, TX

ABSTRACT

This paper reports on the design and implementation of a process, temperature and supply compensated 7-MHz clock oscillator in a 0.25 μ m, double poly, 5-metal CMOS process. The clock generator is based on a 3-stage differential ring oscillator. The compensation technique incorporates a unique combination of a process corner sensing scheme and a temperature compensating network to appropriately change the control voltage of the differential ring oscillator. Measurements made across a temperature range of -40°C to 125°C and 64 samples collected over 3 runs indicate an average variation of $\pm 0.82\%$ ($\pm 46\text{ppm}/^{\circ}\text{C}$) in the clock frequency with temperature, $\pm 2.1\%$ with process across chips at room temperature, and a worst-case combined variation of $\pm 2.6\%$ (with process, temperature and supply). The variation of frequency with power supply was $\pm 0.31\%$ for a supply voltage range of 2.4-2.75V. The measurement results are in good agreement with the simulation results. The oscillator is intended to serve as a start-up clock for micro-controller applications.

1. INTRODUCTION

High precision clock generation is an important requirement for a majority of digital circuits. A micro-controller typically depends on a crystal oscillator to generate a start-up clock. Though crystal oscillators provide excellent stability with variations in supply voltage, temperature and process, their incompatibility with on-chip integration increases the size and the cost of the overall system. Popular integrated circuit techniques for on-chip frequency references include BiCMOS multi-vibrators [1,2] that can offer excellent temperature stability. However, they typically consume large amounts of power and also cannot be implemented in a standard digital CMOS process. The biggest challenge in creating on-chip frequency references in CMOS is to achieve frequency stability with variations in process, temperature, and power supply. Previous approaches that address these issues [3,4] offer solutions that partly solve the problem, but do not address simultaneous compensation for changes in the process, temperature and supply voltage.

Our work reports on a ring-oscillator-based clock generator designed in a 0.25 μ m CMOS process that includes an on-chip voltage regulator and a unique combined temperature and process compensation circuit. Further, the system also employs a process-independent voltage comparator at the output stage to produce a standard digital clock. This oscillator is intended to serve as a start-up clock for a micro-controller, enabling it to program or read an internal flash memory and hence providing the user the ability to configure options on the controller from programmable memory. Simulation and measurement results indicate an overall

variation of only about $\pm 2.6\%$ over a 165°C temperature range across 64 die samples, which to the best of our knowledge is better than any results reported in the literature.

2. SYSTEM ARCHITECTURE

Figure 1 shows the block diagram of the oscillator system. A Band-gap referenced voltage regulator is used to generate a supply and temperature independent reference voltage, V_{REF} . This serves as a stable temperature independent supply voltage for the oscillator and the supporting circuits. The system uses a voltage controlled differential ring oscillator to generate a reference frequency. In the frequency compensation circuit, a threshold voltage sensing circuit generates a process-dependent reference voltage from V_{REF} , which is supplied to the temperature compensating circuit. The output of the compensation circuit is a control voltage, V_{CTRL} , which stabilizes the frequency of oscillation by varying a reference current, I_{REF} . The output of the oscillator is converted to a full swing rail-to-rail clock signal by a process independent voltage comparator [6] to make it compatible with standard logic and increase the noise immunity. The comparator also ensures that the clock duty cycle stays at 50%.

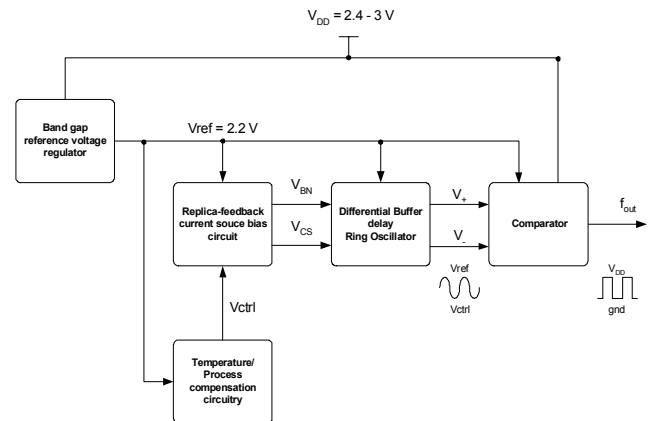


Figure 1. System block diagram

3. CIRCUIT BLOCKS

A. Oscillator and Bias Generator

The reference frequency is created using a ring oscillator configuration with three differential delay stages as shown in Fig. 2. Since a digital compatible output was sought, a comparator was included at the output of the final stage. To eliminate the asymmetric loading of the delay stages caused by the comparator, buffer and dummy delay stages were used. The individual delay

stages consist of a source coupled pair and a symmetric load as shown in Fig. 3 [5]. The time delay produced by the circuit is given by:

$$t_d \approx \frac{C_o(V_H - V_L)}{I_{ref}} \quad (1)$$

C_o is the total capacitance seen at the output of each stage. I_{ref} is the bias current of the circuit and $V_H - V_L$ is the output voltage swing. V_H and V_L are equal to V_{REF} and $V_{LOW}(=V_{CTRL})$ respectively. The time delay can be adjusted by changing the bias current and/or the output voltage swing, which can be accomplished by changing V_{CTRL} .

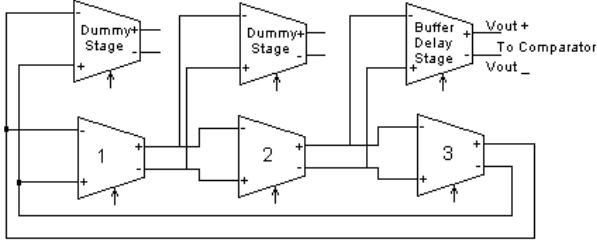


Figure 2. Schematic of the differential ring oscillator

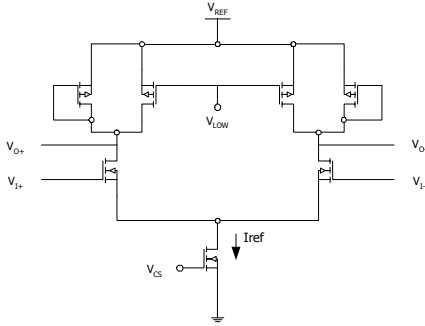


Figure 3. Differential buffer delay circuit

The bias generator for the oscillator is the replica feedback current source bias circuit [5] as shown in Fig. 4. The circuit changes the lower rail voltage by changing V_{CTRL} to maintain the correct delay time under all conditions. The relationship between the control current and V_{CTRL} can be derived from Fig. 4:

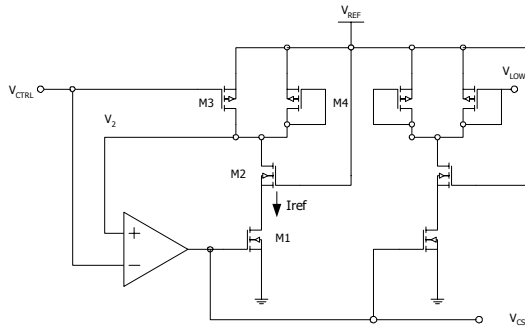


Figure 4. Replica feedback current source bias circuit

$$I_{ref} = g_{m1}(V_2 - V_{ctrl}) \cdot A_v \quad (2)$$

where A_v is the gain of the amplifier, which can be realized as a MOS differential pair, and g_{m1} is the transconductance of M1. Assuming a high gain amplifier and a high (W_1/L_1) ratio in the bias circuit, equation (2) can be simplified as:

$$I_{ref} \approx K'_4 \frac{W_4}{L_4} (V_{ref} - V_T - V_{ctrl})^2 \quad (3)$$

By combining equations (1) and (3), the frequency of oscillation can be expressed as a function of V_{CTRL} :

$$f = \frac{1}{N \cdot t_d} = \frac{K'_4 \left(\frac{W_4}{L_4}\right) (V_{ref} - V_T - V_{ctrl})^2}{N \cdot C_o \cdot (V_{ref} - V_{ctrl})} \quad (4)$$

B. Comparator

The comparator shown in Fig. 5 is used to convert the differential input signal of the ring oscillator to a single-ended, digital logic compatible output voltage with a full ground to supply swing. We used a process-independent threshold inverter-comparator [6], consisting of a common drain input buffer to minimize the loading capacitance seen by the ring oscillator, a source coupled pair configuration to amplify and convert the differential voltage input to single-ended output and the inverter-comparator. The comparator maintains the duty cycle of the output at 50%.

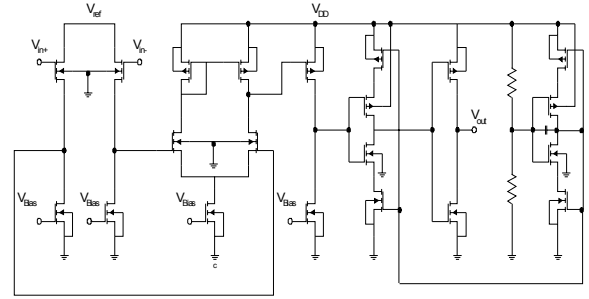


Figure 5. Schematic of process-independent inverter-comparator.

C. Voltage Regulator

The voltage regulator provides the system a temperature and supply independent reference voltage and power supply. The circuit, which is shown in Fig. 6, is primarily divided into two sub-circuits: A bandgap reference with stacked CMOS topology [7], and a feedback transconductance amplifier that raises the output of the bandgap circuit from 1.25V to 2.2V (through the action of the $R5$ - $R6$ feedback loop). A vital feature of the circuit is the low temperature coefficient (in the order of a few-tens of ppm/ $^{\circ}$ C); the rest of the system works on the assumption that the variation of V_{REF} with temperature is negligible.

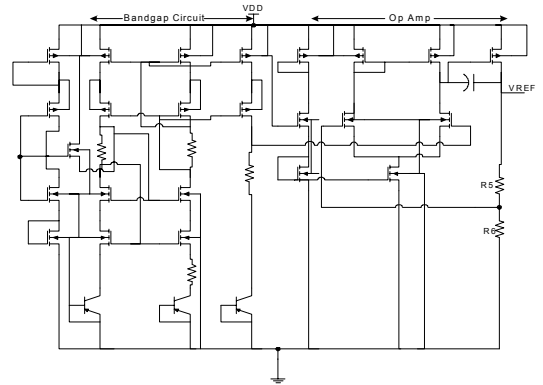


Figure 6. Schematic of the voltage regulator circuit

D. Compensation Circuit

The critical parameters that vary with temperature are the mobility of the charge carriers and the threshold voltage. The relationship governing the variation can be approximately given by [8,9]:

$$\mu_p \propto T^{-2.2} \quad (5)$$

$$V_T(T) = V_{T0} - K(T - T_0) \quad (6)$$

Process variation is mainly due to variations in gate oxide thickness and doping concentrations. These change the threshold voltage and the K' of the MOS transistor. As a result, the oscillating frequency shifts with process even if the system is compensated for temperature variations.

By rearranging (4), one can get the following relationship between V_{CTRL} and f (the oscillator frequency):

$$V_{ctrl} = V_{ref} - V_{TP} - \frac{1}{2} \cdot \frac{f \cdot N \cdot C_0}{K_4' \left(\frac{W_4}{L_4}\right)} - \frac{1}{2} \sqrt{4 \cdot V_{TP} \cdot \frac{f \cdot N \cdot C_0}{K_4' \left(\frac{W_4}{L_4}\right)} + \left(\frac{f \cdot N \cdot C_0}{K_4' \left(\frac{W_4}{L_4}\right)}\right)^2} \quad (7)$$

The second term inside the square root is at least 10 times smaller than the first term for the given conditions of f , N and C_0 and hence can be neglected. The goal is to keep the oscillation frequency (f) constant. By using (5) and (6) in (7), V_{CTRL} can be expressed as a function of temperature:

$$V_{ctrl} \approx A - \frac{B}{T^{-2.2}} - \frac{C}{T^{-1.1}} \quad (8)$$

where A , B , and C are temperature-independent parameters that vary with process corners. For the choice of f , N and C_0 , B is at least 10 times smaller than C , and (8) can be further simplified as:

$$V_{ctrl} \approx A' - C' \cdot T \quad (9)$$

Therefore, in order to compensate for temperature variations, the slope of the control voltage versus temperature should be negative; this can be supplied by V_{BE} of a BJT. However, in order to simultaneously achieve process compensation, equation (9) must be satisfied for all process conditions.

The simultaneous compensation of process and temperature variations is achieved by detecting the process corner using a threshold voltage sensing circuit and using that information to create a process-dependent voltage reference for the temperature compensation circuit. Figure 7 shows the schematic of the complete compensation circuit. The part of the circuit to the left provides a temperature independent current source. The threshold voltage sensor circuit (a diode-connected PMOS) thus provides a voltage that varies significantly only with the process. The op-amp buffer stage boosts this reference level to V_{TREF} (2.2V under typical conditions). The control voltage generator (shown as a part of Fig. 7) is implemented using a diode connected PNP transistor at the bottom rail, providing an output voltage with a negative temperature coefficient. The slope of the V_{CTRL} can be adjusted through W/L ratio of the PMOS transistor on the top rail. It should be noted that V_{CTRL} tracks process variations through changes in V_T , gate oxide thickness and the mobility, and hence does not depend on a change in V_T alone to achieve process compensation.

Assuming a constant frequency, plots of V_{CTRL} versus temperature were generated from simulation for various process conditions. The optimal values for the size of the transistor and the resistor were then generated through the best possible curve fit. It was further determined that better compensation can be achieved by

obtaining a larger change in V_{CTRL} with process (to obtain a better curve fit), which can be implemented by a simple cascade of two of the existing stages. The V_{CTRL} generator was hence modified to that of Fig. 8, resulting in a 2.5X improvement in the frequency stability (confirmed in [simulation](#) and [measurement](#)). Figure 9 shows the required and curve-fit implemented plots of V_{CTRL} versus temperature for various process conditions. It can be seen that the enhanced compensation circuit (Fig. 8) does provide an excellent fit to V_{CTRL} for all process conditions. The results for mixed process corners have not been provided here, since they are highly unlikely to occur [10] and even if they do occur, the frequency variation is less than that of the extreme conditions.

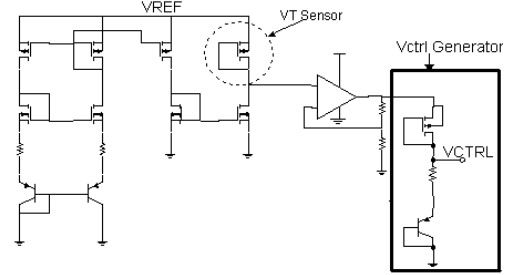


Figure 7. Schematic of the compensation circuit

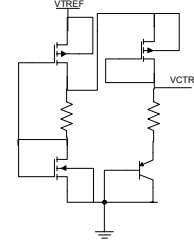


Figure 8. The enhanced compensation scheme

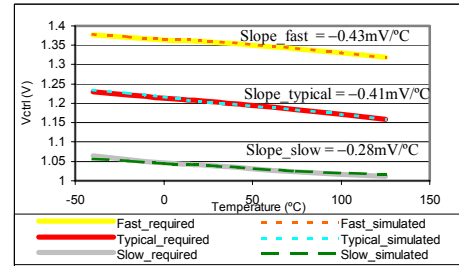


Figure 9. Required and simulated V_{CTRL} vs temperature plots

4. MEASUREMENT RESULTS

The oscillator system was implemented in a 0.25 μ m CMOS process offered by National Semiconductor Corporation. A total of 64 die samples of the designed oscillator system collected from 3 different runs have been tested for performance over a temperature range of -40°C to 125°C . The clock oscillator demonstrated a worst-case variation of $\pm 2.6\%$ in its output frequency (7.03MHz) over the 165°C temperature range and across the 64 die samples. Table 1 provides a summary of the measurement results from the oscillator system and a comparison of the results with simulation. The measurement results are in good agreement with the simulation results.

Table 1. Comparison of simulation and measurement results

Oscillator Performance	Simulation	Measured
Frequency achieved (MHz)	7.02	7.03
Variation with supply (2.4V-2.75V)	0.2%	0.31%
Average Variation with temp (typical process @ 2.5V, -40°C to 125°C)	± 0.78%	± 0.82%
Variation w/ process (25°C, intra run)	± 1.07%	± 1.12%
Variation w/ process (25°C, inter run)	± 1.07%	± 2.12%
Worst case variation (process & temperature – intra-run)	± 1.71%	± 1.7%
Worst case variation (process & temperature – inter-run)	± 1.71%	± 2.62%
Nominal Duty cycle	49.8%	49.6%
Power Consumption (@ 2.5V)	1.5mW	1.5mW

Figure 10 shows a typical output waveform of the clock generator with a supply voltage of 2.4V. It can be seen that the signal swing is almost rail-to-rail and the frequency is right at the target value. Further, the rise and fall times are quite small and the duty cycle is close to the target value of 50%.

Figure 11 gives the distribution of the measured frequencies from the mean, at room temperature. It can be seen that the number of samples with frequencies higher than average is slightly greater than the ones with lower than average frequencies. This is due to the fact that the average frequency measured from one of the runs was higher than that of the other samples. Figure 12 shows the variation of the output frequency with temperature (averaged over the 64 samples). Though the system is designed to work with supply voltages in the range of 2.4-5.5V, the process limits the maximum supply voltage to about 2.75V. Hence, measurements could not be made for higher supply voltages.

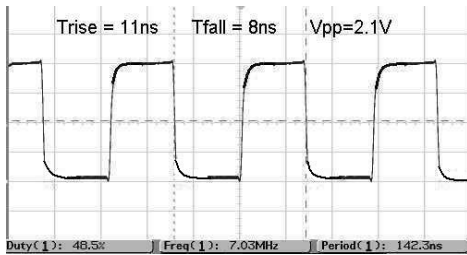


Figure 10. A typical output waveform

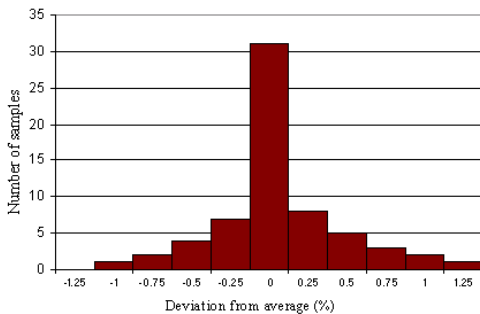


Figure 11. Distribution of frequency measured @ 25 °C

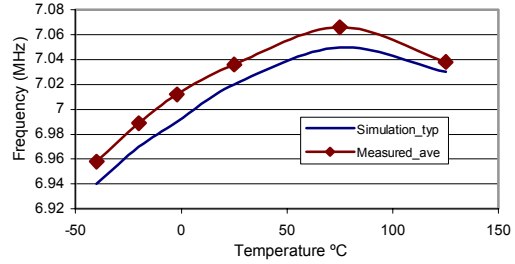


Figure 12. Variation of frequency with temperature

5. CONCLUSION

We have presented a 7-MHz ring-oscillator-based clock generator compensated for variations in supply voltage, temperature and process conditions. The oscillator is implemented in a standard 0.25 μ m CMOS process and the output is compatible with standard digital logic. Measurement results indicate a worst-case variation of $\pm 2.6\%$ across 64 samples collected from 3 different runs over a temperature range of 165 °C, which is better than any result reported so far in the literature.

6. ACKNOWLEDGEMENT

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7. REFERENCES

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