High-Q RF Passives on Organic Substrates Using a Low-Cost Low-Temperature Laminate Process

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Abstract

This paper reports on a low-cost low-temperature (≤150°C) laminate batch fabrication process for implementation of high-Q RF passive components (inductors and capacitors) in system-on-package (SOP) applications. Using this process, various designs of integrated inductors with Q-factors in the range of 60-180 for Bluetooth/IEEE 802.11b (2.4GHz), GSM1800 (1.8GHz) and GSM900 (900 MHz) communication standards have been implemented on an organic package substrate. For the first time, a maximum Q of 180 was measured for a 4.8nH inductor at 2.0 GHz on an organic substrate with a self-resonance frequency (SRF) of 5.5 GHz within an area of 9mm^2. High-Q inductors and capacitors integrated on low-loss organic package substrates can find numerous RF and microwave SOP applications (such as VCO, IF/RF bandpass filters, LNA, etc), in which IC chips are flip-chip mounted on the package substrate. Integration of passives in organic substrates eliminates the excess cost of assembly, enables miniaturization by allowing for added functionality at the board level, and provides an attractive alternative to higher temperature processes such as ceramic and deposition technologies for high-Q passive implementation.

I. INTRODUCTION

Integration of high performance passives such as inductors, capacitors, frequency references, and filters has been a critical barrier in implementation of integrated mixed-signal microsystems. One of the approaches pursued for integration of mixed signal microsystems on a single platform is the system-on-a-chip (SOC) approach. This approach is aimed at the integration of all the passives into the silicon substrate with the package used primarily for interconnection, power distribution, heat dissipation and mechanical support. The primary disadvantage with this approach is that the losses in the silicon substrate and the thin metallization layers limit the quality factor of the inductors. Quality factors (Q) in the range of 5-15 have been reported for spiral inductors integrated on silicon [1]. Currently, technologies are being developed to integrate passives such as inductors on silicon using non-standard materials and processes that use thicker aluminum/copper metallization, and high-resistivity silicon and sapphire substrates [2,3]. However, the increase in Q for inductors has not scaled with the increase in processing complexity. An alternative approach for integrating inductors and passives, known as the system-on-a-package (SOP) approach, is to embed inductors that require high Q in the package substrate using a batch fabrication process.

Low-temperature (<900°C) co-fired ceramic (LTCC) [4] and multi-chip module deposition (MCM-D, <500°C) [5] technologies have been used for integration of passives into the package. A 20-layer LTCC process utilizing standard 90μm thick Dupont tapes have been used in [4] to implement inductors. The tapes have a dielectric constant of 7.8 and a loss tangent of 0.0015 at 10 MHz. Typical metal thickness used in this technology is 5-6μm (gold or silver). In [5] sputtered metal layers (3μm thick) are separated by thin spun-on layers of BCB (5μm thick), which has a dielectric constant of 2.65 and a loss tangent of 0.0008. The BCB is stacked on a glass carrier substrate, which has a dielectric constant of 6.2 and a loss tangent of 0.0009.

This paper presents the integration of high-Q inductors in an organic substrate using a low-cost low-temperature (<150°C) laminate batch fabrication process. In this sequential build-up (SBU) process, a low-cost epoxy-based laminate called Dupont's Vialux™, which has a dielectric constant of 3.2 and a loss tangent of 0.015 at 1 GHz, was used as the dielectric layer on top of FR-4 organic substrate. Comparing to the dielectric materials used in LTCC and MCM-D technologies, epoxy-based laminates have a higher loss. However this technology is capable of implementing 17-25μm thick metal lines (compared to the 5-6μm thick lines in LTCC [4] and 3μm thick lines in MCM-D [5]), which helps reduce the DC resistance of the lines and therefore compensates for the loss in the dielectric material.

The paper is organized as follows: the details of the organic process and testbed are discussed in section II. This is followed by section III that provides details on the topologies and design parameters for inductors. A comparison between the different topologies based on the size and performance is made in section III. The performance of integrated capacitors is discussed in section IV, followed by conclusions in section V.

II. The Organic-Based Laminate Fabrication Process

Figure 1 shows the fabrication process flow for the two metal layer organic-based SOP lamination technology. A 700μm thick thick, copper-cladded (9μm thick Cu) FR-4 organic substrate (epoxy-glass fiber composite) was used as the substrate in this process. A 15μm thick photoresist dry film (Dupont, Riston 206) was first laminated on the substrate (@75°C) using vacuum pressure type laminator and patterned using standard photolithography techniques. The first conductor layer (9μm thick Cu) was then patterned by selectively etching the exposed copper in an ammonium hydroxide solution. The photoresist was then stripped off and a 25μm thick photosensitive dielectric epoxy dry film (Dupont, Vialux™, ε_r=3.2 @1GHz) was vacuum laminated on the first conductor layer. This dielectric layer serves as an insulator between subsequent metal layers. The photo-vias in the dielectric layer were opened through (i) exposure to UV light, (ii) post-baking in oven at 110°C for 1hr, (iii) developing in gamma-butyro lactone (GBL), and finally (iv) curing the dielectric polymer at 150°C (the maximum temperature used in this process) for 1.5hr. The 17-20μm thick upper metal layer and the via's between the lower and upper metal layers were then formed through electroless plating of copper seed layer followed by electrolytic copper plating through a 15μm thick photoresist mold. For electroless copper plating, the surface of dielectric polymer was catalyzed through such process steps as swell, etch, neutralize, pre-catalyst, and catalyst

treatment. After plating was completed, the photoresist was stripped off and the underneath copper seed layer was wet-etched in a micro-etch solution.

Multiple metal layers can be fabricated using the laminate process described above; however, two metal layers are sufficient for signal routing and electrical connections. The cross-section of the testbed along with the major design rules used for fabrication of the inductors is shown in Fig. 2. A 700µm thick FR-4 N4000-13™ organic substrate was used for this testbed (available from Nelco with a dielectric constant of 3.7 and loss tangent of 0.015 at 1GHz). Such a thick substrate is ideally suited for microstrip-type inductors which require a reference ground plane beneath the inductor (on the backside of the substrate). All backside ground connections for microstrip type topologies were made using post-process mechanical drilling techniques which allow for through holes ~500µm in diameter. These holes were then filled with silver paste to make the vias conductive. It should be noted that the through holes could alternatively be electroplated to provide backside electrical connections.

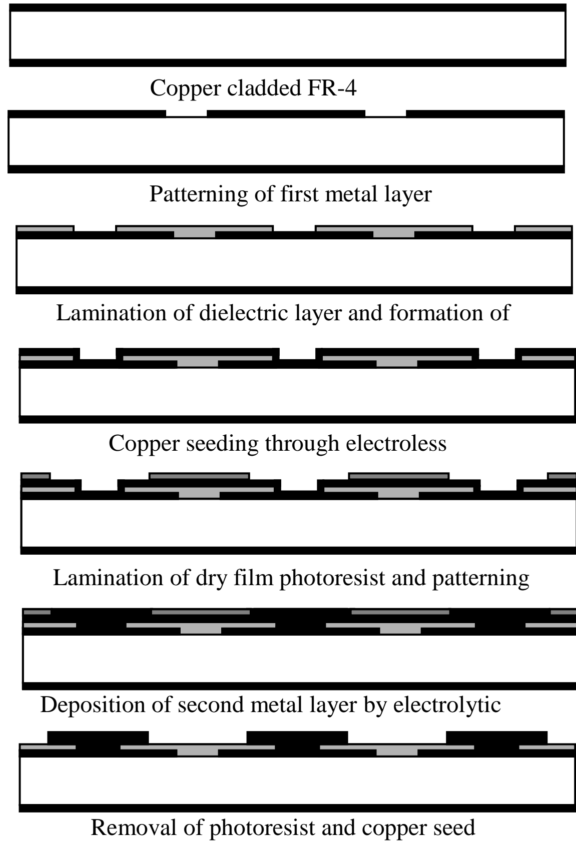


Fig. 1: Process flow for the low-temperature laminate SOP process.

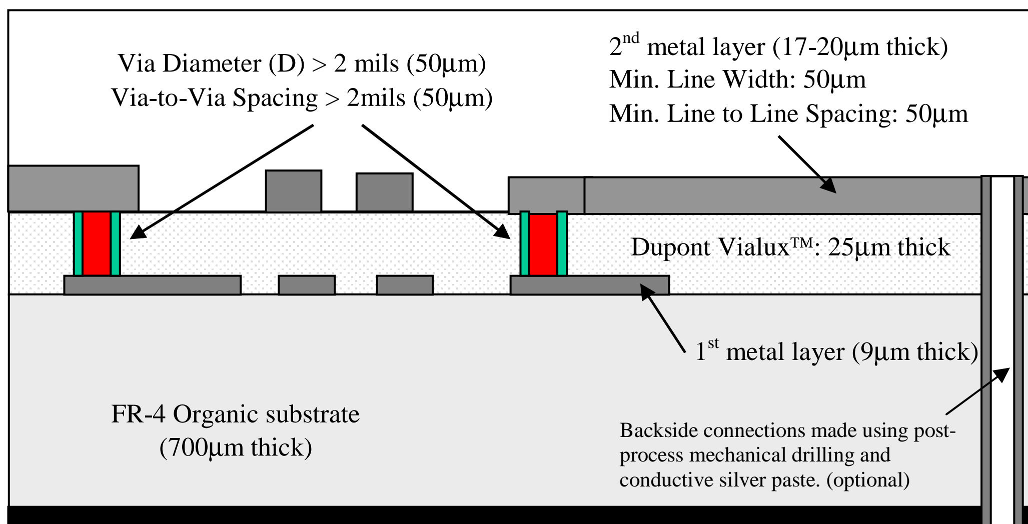


Fig. 2: Cross section of the testbed, showing the major design rules.

III. INDUCTOR TOPOLOGIES AND DESIGN PARAMETERS

Various designs of inductors with spiral and loop topologies were implemented using the laminate organic process. By introducing a ground plane, the spiral and loop topologies can be connected to either microstrip or coplanar waveguide (CPW) configurations. In the microstrip configuration, a ground plane needs to be implemented as a solid metal sheet beneath the current carrying conductors of the inductor, and hence the need for the backside metallization. Unlike the microstrip configuration, a CPW device is implemented by having a wide ground ring around the device, with or without any backside metallization. The trade-offs between these topologies and configurations are explained in this paper. The parameters of interest for the design of inductors are its inductance, Q-factor and self resonant frequency (SRF). The design of inductors can be optimized using a combination of full-wave electromagnetic solvers such as method-of-moment based tools [6] and quasi-TEM approaches [7,8]. Quasi-TEM approaches such as the one mentioned in [7] are faster compared to full-wave solvers and at lower-frequencies (<8GHz) provide a better approximation for the associated loss in devices with thicker metallization (>10μm). However, the approach mentioned in [7] is suitable for inductors with rectangular topologies, since it approximates the device as a series of coupled line sections cascaded to each other via bends and cross-overs. For passives that use a circular topology, full-wave solvers such as SONNET [6] were used for purposes of optimization.

Figure 3 shows the top view of spiral inductors with line widths varying from 7–34mil (175-850μm). The inductors were designed for optimal performance in the 1-2.4 GHz band. Table 1 shows the measured results for the inductors in Fig. 3.

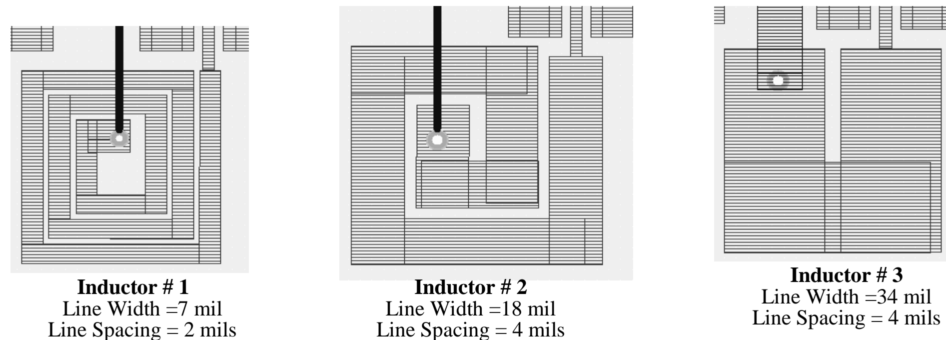


Fig. 3: Spiral inductors implemented on organic substrate

Table 1. Measured data for wide-strip narrow-spacing microstrip spiral inductors shown in Fig. 3.

Inductor	Max Q (Peak Q Frequency)	Effective Inductance	Area	SRF (GHz)
Inductor 1	100 at 1.0 GHz	12nH at 1.0 GHz	3.1mm^2	3.2
Inductor 2	110 at 2.0 GHz	5.2nH at 2 GHz	4.5mm^2	7
Inductor 3	170 at 2.4 GHz	1.5nH at 2.4 GHz	3.2mm^2	8.5

All measurements were done using inbuilt 1 port SOL calibration on HP 8720ES Vector Network Analyzer. An IF averaging factor of 16 with 1601 points for 1GHz of bandwidth was used to perform the measurements. Figure 4 shows the measured plots of Q versus frequency for various microstrip type spiral inductors of Fig. 3. Figure 5 shows the top view of 1-turn (1.5nH) and 2-turn (5.2nH) microstrip inductors fabricated through this process and their cross sectional view (Fig. 5c).

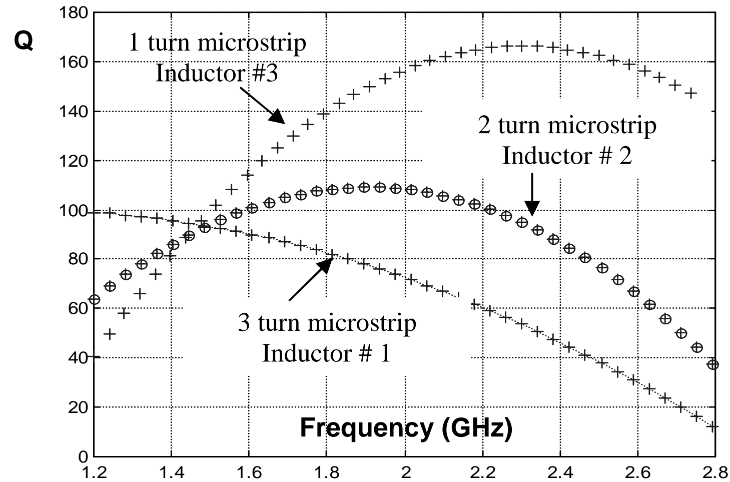


Fig. 4: Measured Qs for inductors # 1, # 2, and # 3 of Fig. 3, versus frequency. Q of ~170 @ 2.4 GHz was measured for a 1-turn microstrip type inductor.

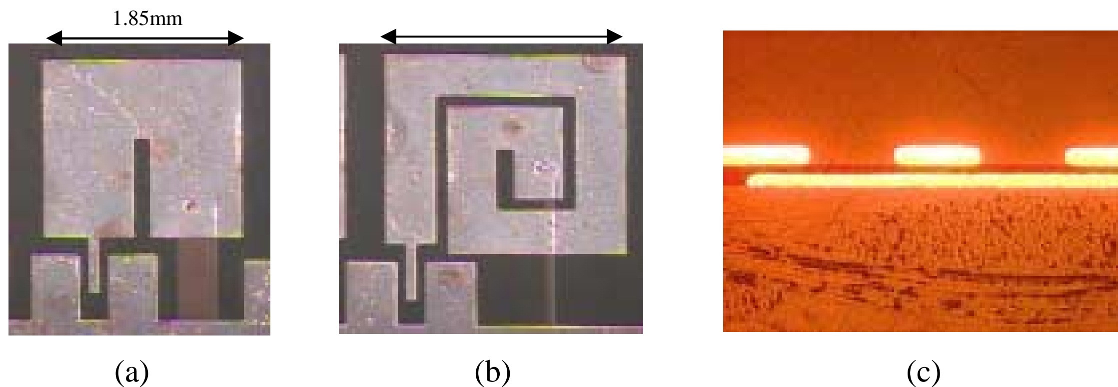


Fig. 5: Microscope pictures of fabricated (a) 1-turn, and (b) 2-turn microstrip-type inductors. (c) cross sectional view of the fabricated inductors, showing the two metal layers and the vialux dielectric layer in between.

Inductors with narrower lines have higher inductance and lower shunt capacitance per line compared to inductor with wider lines. Unlike the narrow-width spirals, wide-strip narrow-spacing multi-turn spirals suffer from eddy current and proximity effects especially in the loops closest to the center of spiral; however, the wide strips and the associated metal thickness (17-20μm) together help reduce the DC resistance significantly compared to narrow-width spiral inductors. Given the above arguments, if a wide-strip and narrow-strip inductor were designed in the same two-dimensional area with the same line-to-line spacings, the narrow-strip spiral would have a much higher

inductance, similar capacitance, lower SRF, and similar resistance (AC+DC) as compared to the wide-strip inductor.

Unlike spiral inductors, loop inductors are inductors in which current carrying loops are cascaded in series and not embedded inside larger outside loops. The primary difference between the spiral and loop topology with the same line width is that the spiral has a higher inductance compared to the loop due to the larger number of positively coupled current carrying segments. In the previous section, narrow-width spirals were modified to wide-strip spirals to obtain the best performance in the 1GHz and 1.8GHz-2.4GHz bands. The advantage with topologies that have narrower lines is that the discontinuities such as bends can be treated as ideal shorts and crossovers between narrower lines have negligible parasitics. Narrower lines do have a higher low frequency resistance, but the proximity and eddy current losses in loop inductors are less compared to wide-strip and narrow-strip spirals. All designs were configured to have adjacent lines carry current in the same direction. Figure 6 shows several microstrip loop inductors with a common ground, which is ~29 mils (28 mils of N4000-13 and 1 mil of Vialux) below the signal lines. Table 2 summarizes the measured data for the loop inductors of Fig. 6. The data was collected using the same method used for spiral inductors. Inductors #4 and #5 are well suited for applications around 2 GHz and inductor #6 is well suited for applications around 1 GHz. Figure 7 shows model to hardware correlation for inductor #4. The modeling was done using the coupled line approach mentioned earlier and described in [7].

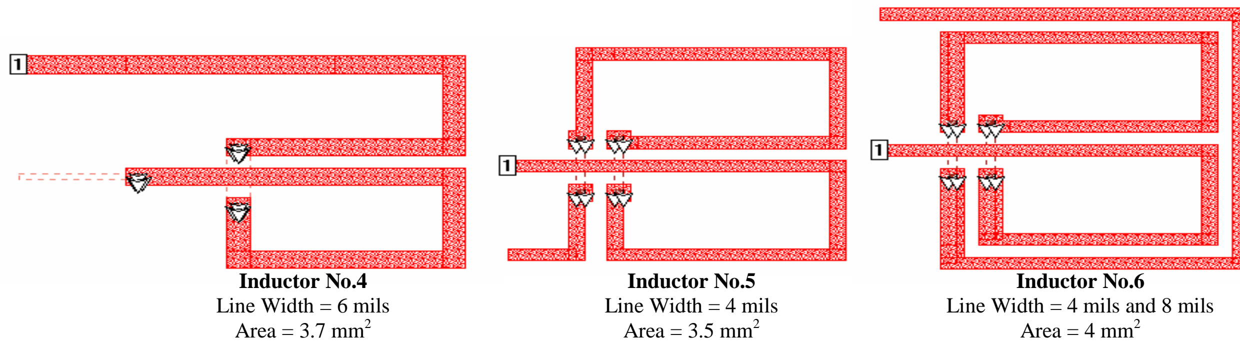


Fig. 6: Microstrip loop inductors fabricated on organic testbed

Table 2. Measured data for Microstrip Loop Inductors shown in Fig. 6.

Inductor	Max Q (Peak Q Frequency)	Effective Inductance	Area	SRF
Inductor 4	Q=110 at 2.1	L=7.8 nH	3.7 mm^2	6 GHz
Inductor 5	Q=85 at 2.2 GHz	L=10.2 nH	3.5 mm^2	5 GHz
Inductor 6	Q=80 at 1 GHz	L=15 nH	4 mm^2	3.2 GHz

Although, both the loop and spiral inductors provided sufficiently high Q factors for the required inductances, their designs require a connection to the backside of the substrate; in other words, without the possibility of having several substrate through holes, referencing other components to the same ground may become a problem during the design stage. Another disadvantage with the microstrip topology at higher frequencies

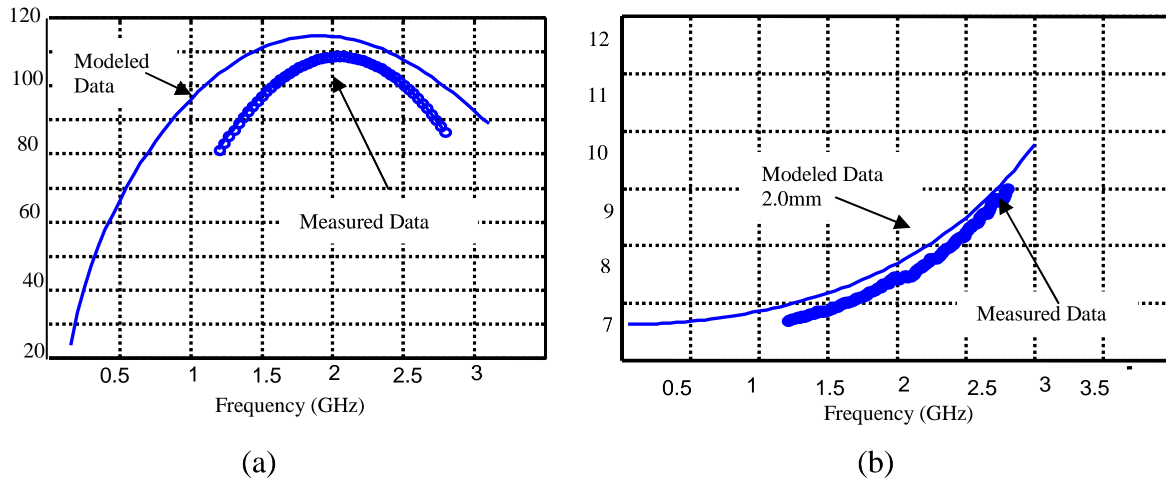
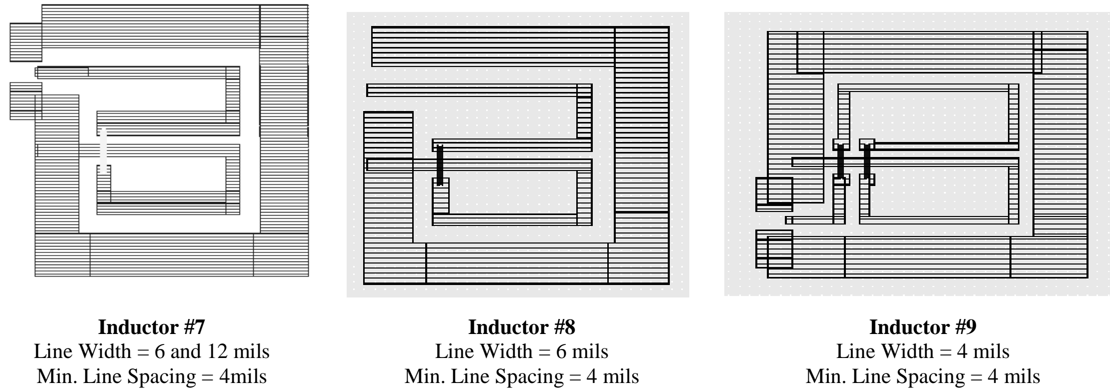


Fig. 7: (a) Q factor vs. frequency for microstrip loop inductor #4; (b) inductance (nH) vs. frequency for inductor #4.

is the current crowding on the ground plane underneath the device. Figure 8 shows several CPW loop inductors that were also implemented on the same organic substrate. Unlike the microstrip inductors, the ground or the reference for the devices are the wide ground rings around the devices as shown in Fig. 8. Although this eliminates the need for backside connections, it does increase the area of the device. The CPW topology ensures the proximity of the ground since the inductor and the ground lines are co-planar, and also prevents the current crowding on the ground planes by forcing the currents to flow around the device on the larger area coplanar ground. Table 3 presents the CPW inductor results measured using the same procedure outlined for the spiral and loop inductors.



Inductor #7
Line Width = 6 and 12 mils
Min. Line Spacing = 4mils

Inductor #8
Line Width = 6 mils
Min. Line Spacing = 4 mils

Inductor #9
Line Width = 4 mils
Min. Line Spacing = 4 mils

Fig. 8: CPW/Hollow-ground loop inductors fabricated on organic substrate.

Table 3. Measured data for CPW loop inductors shown in Fig. 8.

Inductor	Max Q (at Freq [GHz])	Effective Inductance (nH)	Area mm^2	SRF GHz
Inductor 7	Q=180 at 2.2	L = 4.8	9	5.5
Inductor 8	Q=140 at 1.9	L = 5.8	9	5.2
Inductor 9	Q=120 at 1.8	L = 8.8	9.5	5

The achievable Q factors in CPW topology are significantly higher (20-30%) as compared to either of the microstrip topologies. For example, inductor #7 implemented within an area of $9mm^2$ measured a maximum Q of 180 at 2.2 GHz with an effective inductance of 4.8nH which is far more than what is achievable for similar spiral and loop inductors such as #3 and #4 with similar inductances. The primary disadvantage with CPW topology is the increased area of the device. In this work, the size of all CPW inductors was kept to a reasonable maximum of $9mm^2$.

From the arguments presented so far the following conclusions can be made: CPW configuration provides higher Q factors compared to microstrip configuration; narrower lines provide higher inductance per unit length; spiral topologies provide the maximum inductance per unit area; increased spacing between lines helps reduce proximity losses; and increased spacing between ground and inductor lines helps reduce parasitics. Figure 9 shows a narrow width circular spiral inductors implemented in a CPW configuration with a large signal to coplanar ground separation. The circular topology further reduces the loss due to current crowding in sharp corners of the rectangular topology. Although large in size ($25mm^2$), the inductor measured 16nH with a max Q of 160 at 1.8 GHz and SRF>4 GHz. Another circular inductor, with an area of $28mm^3$, measured 9nH with a max Q of 180 at 2.2 GHz and SRF>4.5 GHz.

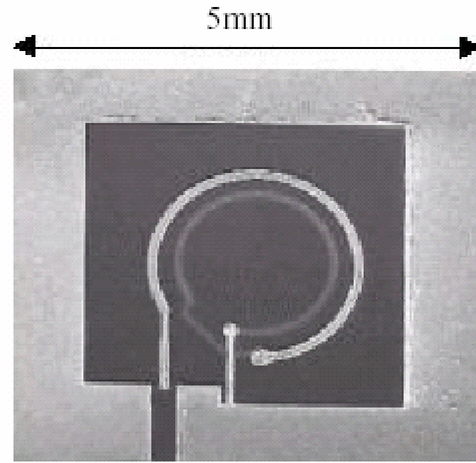


Fig. 9: 2-turn 16nH circular spiral CPW inductor: Q=160 at 1.8GHz

The measured results from the inductors clearly advocate the use of low-temperature organic processes as an attractive alternative to LTCC and MCM-D technologies for integrated inductor applications.

IV. CAPACITORS TOPOLOGIES AND DESIGN PARAMETERS

Several parallel-plate capacitors were also fabricated using this process. Figure 10 shows various capacitors implemented on the testbed shown in Fig. 2, with the 2nd metal layer serving as the feed/signal layer and the 1st metal layer acting as the ground plane. This provides for 25µm of Vialux as the dielectric medium between the plates of the capacitor. In contrast to the inductors where the dominant loss is the conductor loss, in capacitors the loss through the substrate is the dominant loss mechanism. The upper limit of the Q factor for any size capacitor implemented on this substrate at a particular frequency *f*, neglecting the conductor loss, can be approximated by $1/\tan\delta$, where $\tan\delta$ is the loss tangent of the material at frequency *f*. The vendor supplied data for Dupont Vialux is as follows: $\tan\delta=0.015$ at 1GHz and $\tan\delta=0.02$ at 2GHz. This sets an upper limit for the Q of the capacitors of 66 at 1GHz and 50 at 2GHz. This argument is supported by the measured results shown in Table 4. Q factors in the range of 40-60 were obtained for capacitors in the range of 1pF-10pF at 2GHz. The measured results for

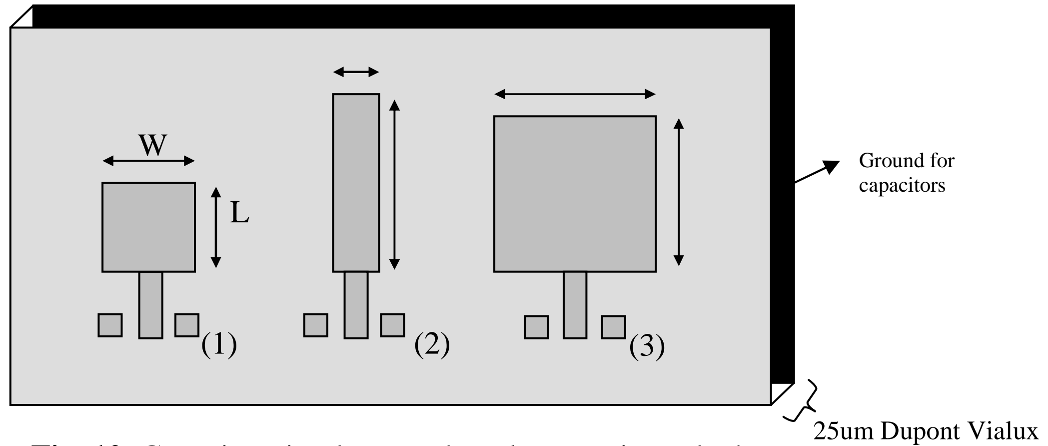


Fig. 10: Capacitors implemented on the organic testbed.

Table 4. Measured Data for capacitors shown in Fig. 10.

Capacitor	Width (W)	Length (L)	Capacitance at 2 GHz	Q at 1 GHz	Q at 2 GHz	SRF (GHz)
Cap #1	30 mils	31 mils	0.92 pF	49	33	6.9
Cap #2	30 mils	60 mils	1.78 pF	42	30	6
Cap #3	58 mils	50 mils	2.72 pF	36	28	5.2

embedded capacitors show the need for lower loss materials to achieve higher Q capacitors. One of the reasons for the popularity of ceramic substrates for embedded capacitor applications is the low loss nature of the materials ($\tan\delta=0.0015$ at 10 MHz [4]). A Q of 90 at 1 GHz and 60 at 2 GHz has been reported for a 1.4 pF capacitor in [4]. The use of lower loss organic laminates such as Teflon ($\tan\delta<0.002$ @ 1GHz) and N6000™ substrate ($\tan\delta<0.008$ @ 1GHz) is currently being investigated for this process.

V. Conclusions

Inductors with maximum quality factors in the range of 60-180 were obtained at frequencies in the 1-3 GHz band for inductances in the range of 1nH to 20nH. These inductors were fabricated on an organic substrate using a low-cost low-temperature (<150°C) laminate batch fabrication process. This is the first demonstration of such high Q inductors in organic substrates. The microstrip loop and spiral inductors with areas <4.5mm^2 and volumes <3mm^3 are ideally suited for integration in compact RF/microwave systems. The CPW inductors, though larger in planar size, offer the advantage of higher Q factors and access to ground reference on the same layer. The increased metal thickness of 17-20µm in this process helps lower the resistive loss of the lines, which is the dominant loss in the inductors. Such a large metal thickness is not currently possible in higher temperature processes such as LTCC and MCM-D. These results advocate the use of low-temperature organic processes as an attractive alternative to LTCC and MCM-D technologies for integrated inductor applications. The advent of lower loss organic laminates such as Teflon ($\tan\delta<0.002$ @ 1GHz) and N6000™ substrate ($\tan\delta<0.008$ @ 1GHz) suggests the possibility of using the same low

temperature low-cost process for high Q embedded capacitor applications in the near future.

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