

# SINGLE-MASK REDUCED-GAP CAPACITIVE MICROMACHINED DEVICES

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## ABSTRACT

This paper presents single mask capacitive micromechanical devices with dry-etched deep-sub-micron gaps. Thick oxide mask layer with sub-micron openings suitable for etching deep narrow trenches is fabricated using a gap-reduction technique. Less than 100nm openings are realized while the original feature sizes are defined by conventional optical lithography. This method combined with modified high aspect ratio DRIE recipes shows a great potential for batch-fabrication of high-frequency low-impedance single crystal silicon resonators on SOI substrates. Results measured from various resonator structures with frequencies as high as 205 MHz, Q values as high as 68,000, and 200nm gaps with aspect ratio of 60:1 are demonstrated.

## 1. INTRODUCTION

Deep-sub-micron vertical gaps are required in certain MEMS devices to increase the capacitive electromechanical coupling. Higher coupling results in higher signal to noise ratio in sensors [1] and lower equivalent motional impedance in electromechanical resonators [2]. Most of the previously reported processes capable of defining deep-sub-micron gaps are multi-mask fabrication sequences involving multiple deposition/etching steps. In these processes gaps are usually defined by the thickness of a sacrificial layer [2,3]. As DRIE techniques improve and higher aspect ratio trenches with smaller width become achievable, dry-etching of trenches for implementation of sub-micron capacitive gaps becomes increasingly attractive. This will potentially simplify the fabrication process and enable implementation of all single crystal silicon devices. However, there are some challenges. Mask formation for dry-etching of sub-micron feature sizes is not trivial and demands for expensive state of the art optical lithography equipments. The other limiting factor is the selectivity of the etching process to the mask material. The trench depth, assuming availability of very high aspect ratio etching processes ( $AR > 50:1$ ), can be restricted by the mask thickness and not necessarily by the aspect ratio of the etch process.

In order to overcome these limitations, application of sacrificial polysilicon deposited on the sidewalls of a trench etched in oxide was studied in our group and dry-etched narrow vertical gaps in silicon were reported successfully [4]. However, our previous work was mainly targeted towards demonstration of deep-sub-micron trench etching using the Bosch process, and could not really simplify the fabrication process flow of arbitrary-shaped devices. It required three masking steps, and trenches would only appear in single-size adjacent pairs, limiting its applicability. The work presented here is the first single mask process that effectively enables low-cost

implementation of high-performance capacitive micro-electromechanical devices with various-size deep-sub-micron gaps.

## 2. DEEP-SUB-MICRON TRENCH ETCHING

### Thick Oxide Mask Formation

The selectivity of the etch process to the masking layer is of great importance, especially when a thick mask layer is neither feasible nor favorable for small feature sizes. Most of the silicon DRIE processes demonstrate higher selectivity to silicon dioxide than organic materials (photoresist). Also, for low temperature cryogenic RIE processes where organics can not be applied due to their cracking problem, oxide is a common choice of masking layer. In order to achieve high aspect ratio structures the oxide mask with sub-micron feature sizes should be thick enough to withstand long DRIE process. In this work, thick layer of oxide with sub-micron features is formed by oxidizing a polysilicon layer with micron-size patterned features. Figure 1 shows a brief schematic diagram of the process flow.

The process begins with the deposition of a thin layer of LPCVD nitride which will prevent the oxidation of silicon layer in subsequent process steps. A thin-film polysilicon layer is deposited and patterned. The smallest feature size on the poly layer is determined by the lithography ( $> 1\mu\text{m}$  typically). Finally the patterned poly will be thermally oxidized in an oxidation furnace to form a thick oxide mask for DRIE step. Meanwhile all the openings are reduced in size due to  $\sim 2$  times enlargement of oxidized polysilicon. The final opening size in this process varies with the thickness of the polysilicon layer and the subsequent oxidation step.

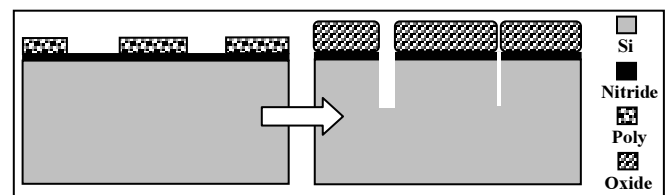


Figure 1: Brief schematic process flow of thick oxide mask formation with various size sub-micron openings (reduced-gap technique).

The enabling features of this technique are:

1- A low-cost oxide mask with deep-sub-micron feature sizes can be batch fabricated using conventional optical lithography equipments.

2- The oxide masking layer with deep-sub-micron openings can be as thick as a few microns which facilitate deep trench etching in subsequent DRIE step.

3- Multi-size sub-micron gaps can be defined in a single step by varying the size of the original openings in the poly mask. This feature is not available in other small gap-formation techniques based on sacrificial layers.

### Trench Etching

The Bosch process is widely used to etch high aspect ratio trenches in silicon. However, standard Bosch recipes are not suitable for etching deep-sub-micron trenches. The isotropic nature of  $\text{SF}_6$  plasma in etching silicon introduces rough, scalloped trench sidewalls and excessive undercut. In deep-sub-micron regime, undercuts and scalloping sizes in the range of 0.1-0.5 $\mu\text{m}$  are not tolerable, as they become comparable in size to the trench width. Numerous approaches have been studied to reduce the sidewall roughness and increase the aspect ratio of Bosch process [5,6]. All these efforts target highly anisotropic etching step and efficient sidewall passivation. These can be partially accomplished by any of the three following solutions:

1. Increasing the switching frequency of the plasma gases while keeping the cycle time ratio of (etch:passivation) constant. This will reduce the roughness of the sidewalls by decreasing the isotropic etch time at the bottom of the trench before the next passivation step protects the sidewall.

2. Increasing the platen power, which elevates the plasma ions flux and energy, and improves the directionality of the plasma reactive particles. This will increase availability of plasma species at the bottom of a trench with very narrow opening. However, too much increase in platen power causes visible bowing in the trench profile. Elimination of the local bowing has been practiced by introducing oxygen in  $\text{SF}_6$  plasma [7].

3. Reducing the chamber pressure, which increases the mean free path of the plasma particles and improves directionality of energetic ions toward the target surface.

Considering all of the above mentioned parameters, a modified recipe for deep-sub-micron trench etching was developed (table 1) and utilized in a STS Advanced Silicon Etcher (ASE) machine.

Table 1: Bosch process recipe parameters used to etch sub-micron trenches in STS ASE machine.

Etch/ Passivation (second)	Pressure (mTorr)	RF power	Platen power	$\text{SF}_6/\text{O}_2$ flow rate (sccm)
4/3	8	700	30	100/20

A 1.3 $\mu\text{m}$  LPCVD polysilicon was deposited and patterned with 1 $\mu\text{m}$  openings on several wafers. Thermal oxide with different thicknesses was grown to achieve a variety of opening sizes. Results of implementing the etching recipe on these samples showed outstanding improvement in sidewall smoothness and promising aspect ratios ( $>20:1$ ) (Fig. 2). The etch rate is compromised in achieving smooth sub-micron trenches unless improvements is made to plasma density.

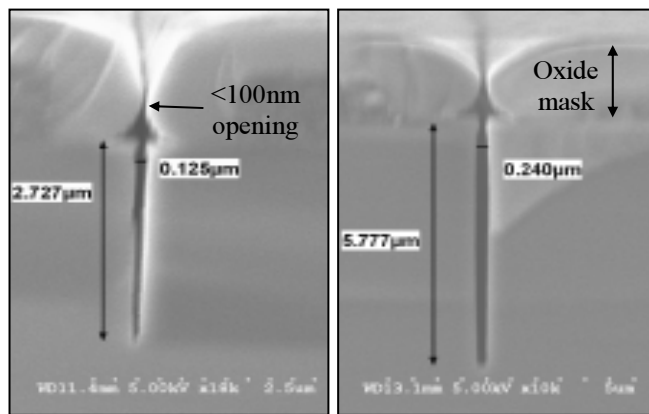


Figure 2: SEM pictures of 125nm and 240nm wide trenches with aspect ratios  $>20:1$  etched in silicon using the modified Bosch recipe.

Further increasing the switching frequency of plasma gases and reducing chamber pressure might facilitate deeper sub-micron trenches. However, instability of pressure at lower values and limitation on switching the gas flow restrict the applicability of this approach. Aspect ratio values greater than 30 are rarely reported using the Bosch process. Inadequate removal of passivation layer at the bottom of the trench as it gets deeper is believed to be the main aspect ratio limiting mechanism.

Optimization of the depassivation step by introducing a third oxygen plasma pulse after the passivation pulse has been studied [8] and implemented in the new DRIE machine (AMS 200) manufactured by Alcatel. Sub-micron trenches with aspect ratios as high as 60 has been demonstrated using the so called SHARP (Super High Aspect Ratio Process) process [9].

The efficiency of SHARP process to etch trenches on the wafers covered with 0.8 $\mu\text{m}$  thick oxide masks and 200 nm opening size fabricated using the reduced-gap process was investigated. As shown in Fig. 3, 200nm wide trenches with aspect ratios as high as 60 have been achieved for  $\sim 12$  minutes process time. Due to the limited silicon to oxide selectivity of the process ( $\sim 20:1$ ) thicker oxide is required to perform longer process time.

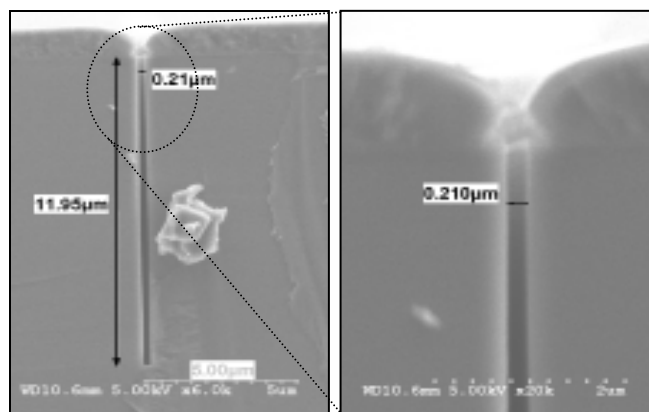


Figure 3: SEM picture of 12.3 $\mu\text{m}$  deep 210 nm wide trenches etched in ALCATEL AMS 200. (AR $\sim 60:1$ )

### 3. SINGLE MASK DEVICES ON SOI

The oxide mask formation technique proposed in this paper offers a method for creating various sub-micron as well as micron-size openings using a single optical patterning step. This feature enables fabrication of capacitively-transduced MEMS devices using a single mask process on SOI. Figure 4 shows a schematic process flow. The process is the same as what was described earlier in the paper to create the oxide mask. Trenches are etched down to the BOX layer of the SOI substrate. The oxide and nitride layers will be removed and finally a wet HF release step is performed.

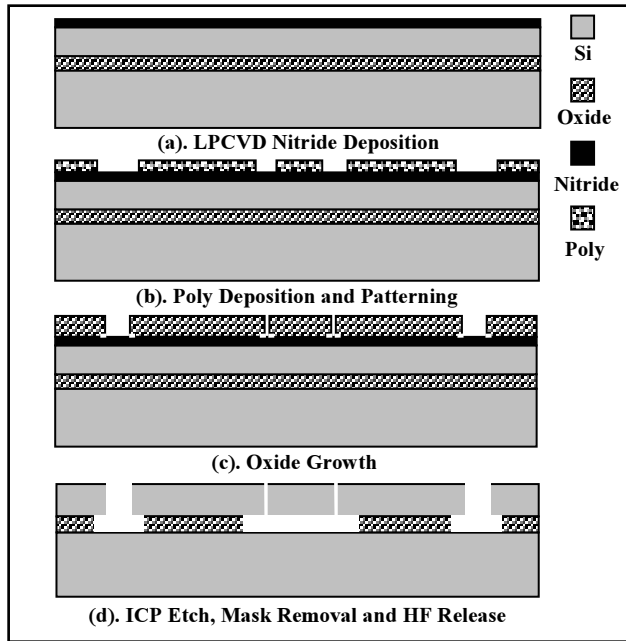


Figure 4: Schematic process flow of single-mask reduced-gap process.

To evaluate the performance of this reduced-gap single mask process, electromechanical resonators were fabricated and tested. Various resonators with different structural designs were drawn on the mask to cover a broad range of frequency and quality factor. Both modified Bosch and SHARP recipes were utilized in different batches. Figures 5 and 6 show fabricated resonators.

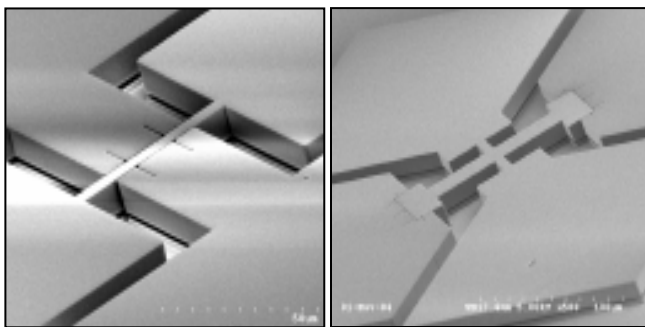


Figure 5: SEM pictures of 50µm long, 6µm wide and 10µm thick beam resonator fabricated using modified Bosch process and 140µm long, 5µm thick I-block resonator fabricated using SHARP process.

Unlike the processes that create small gaps by removal of sacrificial oxide layer, the HF release step in this process is short (enough to remove the oxide beneath the movable structure). For very wide structures, some release holes were considered in the resonator body to reduce excessive HF release time (Fig. 6). Measurement results presented in the following section showed very minor effect on frequency caused by introducing the release holes in the bulk mode resonator. A zoom-in picture from resonator sidewall in Fig. 6 shows very little scalloping introduced in DRIE etch step.

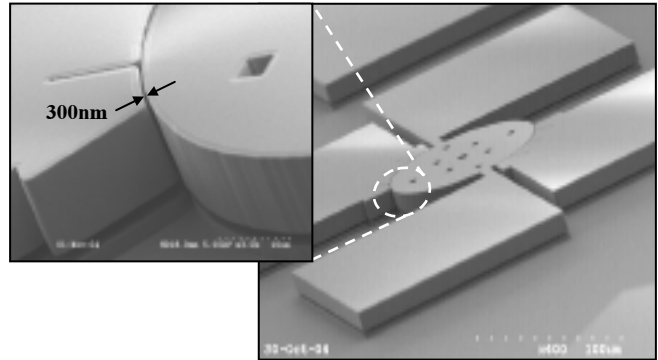


Figure 6: SEM picture of 100µm in diameter side-supported disk resonator on a 10µm thick SOI wafer.

### 4. TEST RESULTS

Frequency response of fabricated resonators with different structures were measured using a network analyzer in two-port configuration.

Highest recorded resonant frequency was 205 MHz measured for a 20µm wide, 10µm SiBAR [10] resonator (fig. 7). Comparing the measured motional impedance of this device at 50V polarization voltage with the one presented in [10], an effective capacitive gap size of ~260nm is extracted.

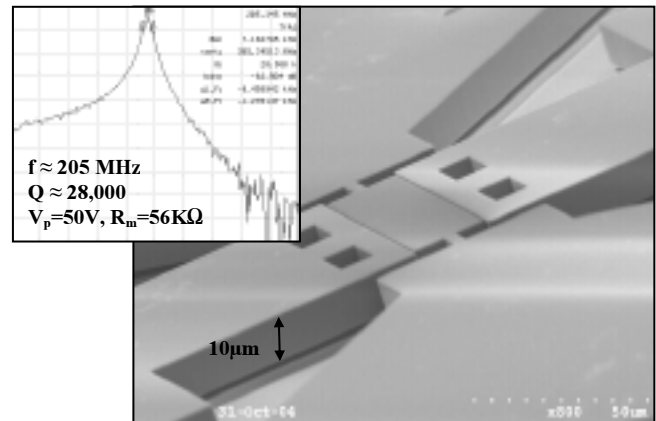


Figure 7: SEM picture and frequency response plot from 20µm wide, 80µm long SiBAR[10] resonator.

Highest quality factor was measured to be ~68,000 at resonant frequency of 21.4MHz for the 140µm long I-block resonator of (fig. 5) in vacuum. The two extended areas on either ends (resembling the I shape) of this block resonator are designed to provide more transduction capacitance and reduce the motional impedance of the resonating structure

[11]. Figure 8 shows two resonant peaks measured from two 140 long I-block resonators with support beams that are different in size. The resonant frequencies are almost the same (~21.4MHz) but quality factor of the one with wider support beam is more than 3 times lower than the other one. This observation confirms that the measured quality factor for these structures is mainly limited by support loss.

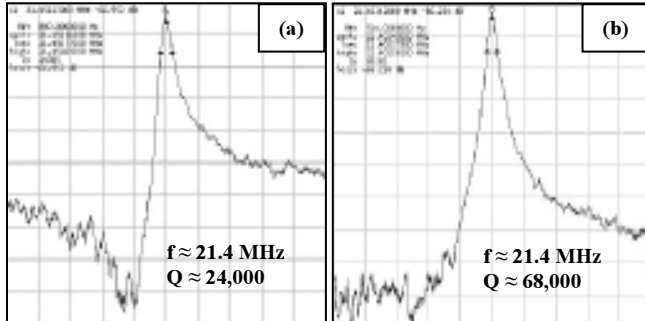


Figure 8: frequency response plots showing 21.4 MHz resonance peaks measured from 140 $\mu$ m long I-block resonators with a) 20 $\mu$ m (l) x 10 $\mu$ m (w) and b) 20 $\mu$ m (l) x 6 $\mu$ m (w) support beams.

Measured quality factors of Fig. 9 for the beam resonator of Fig. 5 and side-supported disk resonator of Fig. 6 were also confirmed to be limited by support loss when compared with the estimated Q-support values obtained through expressions in [12,13].

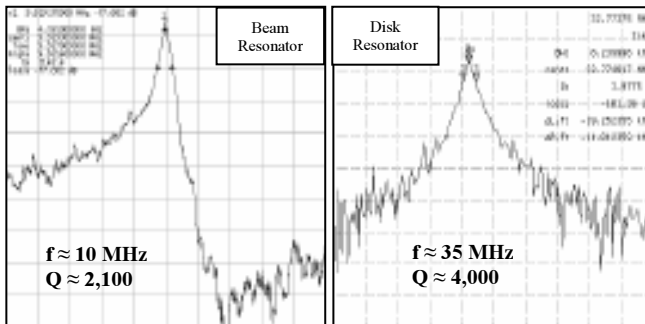


Figure 9: frequency response plots measured from the beam resonator of figure 5 and the disk resonator of figure 6.

Figure 10 shows the frequency versus temperature plot for the I-block resonator of figure 5. The TCF value extracted from this plot is ~ -24.8 ppm/ $^{\circ}$ C.

## 5. CONCLUSION

A simple cost effective single-mask process to fabricate thick oxide masks with deep-sub-micron openings was presented. Modified Bosch and SHARP recipes were implemented to fabricate fully single crystal silicon resonating structures with narrow dry-etched capacitive transduction gaps. Results from fabricated devices were presented and measured quality factor values verified to be limited by support loss to a large extent.

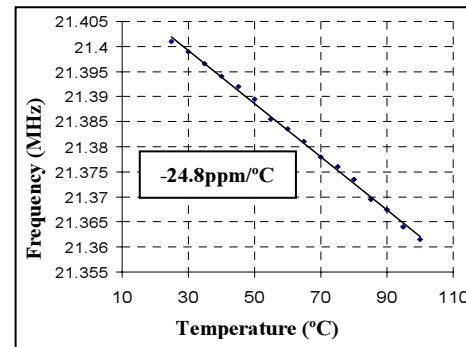


Figure 10: Frequency vs. temperature plot for I-block resonator of figure 5.

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## REFERENCES

- [1] B. Vakili Amini, *et al.*, "A High Resolution, Stictionless, CMOS Compatible SOI Accelerometer with a Low Noise, Low Power, 0.25 $\mu$ m CMOS Interface", in *proceeding of IEEE MEMS'04*, Jan. 2004, pp. 572-575
- [2] S. Pourkamali, *et al.*, "18 $\mu$ m Thick High Frequency Capacitive HARPSS Resonators with Reduced Motional Resistance", in *Solid-State Sensors, Actuators, and Microsystems Workshop*, Hilton Head, SC, June 2004, pp. 392-393
- [3] J. R. Clark, *et al.*, "High-Q VHF Micromechanical Contour-Mode Disk Resonators", *IEEE IEDM*, San Francisco, California, Dec. 11-13, 2000, pp. 399-402.
- [4] S. Pourkamali, and F. Ayazi, "Fully Single Crystal Silicon Resonators with Deep-Submicron Dry-Etched Transducer Gaps", *IEEE MEMS '04*, Jan. 2004, pp 813-816
- [5] B. Volland, *et al.*, "Dry Etching with Gas Chopping without Rippled Sidewalls", *J. Vac. Sci. Technol. B* 17(6), Nov./Dec. 1999.
- [6] M. Chabloz, *et al.*, "Improvement of Sidewall Roughness in Deep Silicon Etching", *Microsystem Technologies* 6, 2000.
- [7] C. K. Chung, *et al.*, "High Aspect Ratio Silicon Trench Fabrication by Inductively Coupled Plasma", *Microsystem Technologies* 6, 2000.
- [8] M. A. Blauw, *et al.*, "Advanced Time-Multiplexed Plasma Etching of High Aspect Ratio Silicon Structures", *J. Vac. Technol. B* 20, 2002.
- [9] M. Puech, *et al.*, "A Novel Plasma Release Process and a Super High Aspect Ratio using ICP Etching for MEMS", *SEMICON*, Japan, Dec. 2003.
- [10] S. Pourkamali, *et al.*, "Vertical Capacitive SiBARs", *MEMS'05*, Miami, 2005.
- [11] G. K. Ho, *et al.*, "Low-Motional-Impedance Highly-Tunable I<sup>2</sup> Resonators For Temperature-Compensated Reference Oscillators", *MEMS'05*, Miami, 2005.
- [12] Z. Hao *et al.*, "An Analytical Model for Support Loss in Micromachined Beam Resonators with In-plane Flexural Vibrations", *Sensors and Actuators A*, Vol. 109, Dec. 2003, p.156.
- [13] Z. Hao and F. Ayazi, "Support Loss in Micromechanical Disk Resonators", *MEMS'05*, Miami, 2005.