

**GEORGIA INSTITUTE OF TECHNOLOGY**  
**School of Electrical and Computer Engineering**

**ECE6412**

**ANALOG INTEGRATED CIRCUIT DESIGN II**

**Spring 2006**

**COURSE INFORMATION**

**Course Instructor:** Professor Farrokh Ayazi  
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**E-mail address:** [ayazi@ece.gatech.edu](mailto:ayazi@ece.gatech.edu)  
**Lectures:** MWF 11:05-11:55 AM VL C457  
**Office Hours:** M 12-1PM and W 1-2PM in MiRC 204, or by appointment  
**TA:** Mina Rais-Zadeh (minaii@ece.gatech.edu)

**TEXT:**

**Required text:** *Analysis and Design of Analog Integrated Circuits*, by Gray, Hurst, Lewis and Meyer, 4<sup>th</sup> edition, Wiley, 2004

**Strongly Recommended:** *CMOS Analog Circuit Design*, by Allen and Holberg, Oxford University Press, 2002.

**WWW:**

The official class website is at: <http://www.ece.gatech.edu/research/integrated-mems/courses/courses-ECE6412.htm>. You can download homework and homework solutions from the website.

You can also download pdf copies of classroom material from previous offerings of the course (by Prof. Phil Allen) at his academic website: <http://users.ece.gatech.edu/~pallen/Academic/>

**PREREQUISITES**

ECE 4430 (Analog Integrated Circuit Design I), or permission of the instructor

**COURSE DESCRIPTION**

The purpose of this course is to enable the student to model, analyze and design analog integrated circuits using bipolar and/or MOS technologies. At the conclusion of the course, the student should be able to successfully perform the electrical and physical (layout) design and simulation of an op amp or analog circuit of similar complexity in an industrial environment.

**GRADING POLICY**

This course will consist of three midterm exams (50 minutes each) and a comprehensive final exam. Grades will be determined based on the following:

- **Homework:** 10%
- **Midterm Exams:** 60%
- **Final Exam:** 30% (Fri May 5<sup>th</sup>, 2:50-5:40PM)

**COMPUTER SIMULATION**

Students are expected to be able to use HSPICE for classroom assignments. Most assignments using the computer will work on the student version of PSPICE.

**WEEKLY COVERAGE OF TOPICS FOR ECE6412 (SPRING 2006)**

<b>Week</b>	<b>Date</b>	<b>www lecture</b>	<b>Topic</b>	<b>GHLM</b>	<b>AH (Chp 5-8)</b>
1	1/9 1/11 1/13	010 020 030	ECE 4430 review (MOS and BJT models) ECE 4430 review (Bipolar & CMOS IC technology) ECE 4430 review (Basic amplifier circuits)	Chapter 1 Chapter 2 Chapter 3	
2	1/16 1/18 1/20	040-050 040-050	Holiday Current mirrors Differential pair w/ active load	Chapter 4 Chapter 4	
3	1/23 1/25 1/27	050 060 070-080	Output Stages Output Stages Single stage frequency response	Chapter 5 Chapter 5 Chapter 7	
4	1/30 2/1 2/3	080-090 100 110-120	Single and Multiple stage frequency response Multiple stage frequency response Op Amp Intro	Chapter 7 Chapter 7 Chapter 6	Chapter 6
5	2/6 2/8 2/10	120-130	Exam 1 preparation session <b>EXAM # 1</b> Compensation of two stage Op Amps	Chapter 9	Chapter 6
6	2/13 2/15 2/17	130-140 140-150 160	Compensation of two stage Op Amps Simple CMOS and BJT Op Amps MOS Op Amp design	Chapter 9 Chapter 6 Chapter 6	Chapter 6
7	2/20 2/22 2/24	170 180 190	Intuitive analysis of analog IC's Power Supply Rejection Ratio (PSRR) Cascode Op Amps I		286-293 293-309
8	2/27 3/1 3/3	190-200 210-220 220-230	Cascode Op Amps II (Folded and Active) Analysis of 741 Op Amp I Analysis of 741 Op Amp II	Chapter 6 Chapter 6 Chapter 6	293-309
9	3/6 3/8 3/10	250-260	Exam 2 preparation session <b>EXAM # 2</b> Feedback I	Chapter 8	
10	3/13 3/15 3/17	260-270 270-280 290	Feedback II Feedback III Feedback IV (Return Ratio Analysis)	Chapter 8 Chapter 8 Chapter 8	
11	3/20- 3/24	Spring Break			
12	3/27 3/29 3/31	310 310 310	Frequency response & stability of feedback amplifier Frequency response & stability of feedback amplifier High speed/frequency OpAmps	Chapter 9 Chapter 9 Chapter 9	368-384
13	4/3 4/5 4/7	320 320-300 300	Differential output OpAmps Differential output OpAmps / Buffered OpAmps Buffered OpAmps/ Switched Capacitor	Chapter 12 Chapter 12,5 Chapter 5	384-393 352-368 352-368
14	4/10 4/12 4/14	340	Exam 3 preparation session <b>EXAM # 3</b> Low noise OpAmps I	Chapter 11	402-414
15	4/17 4/19 4/21	340 330 350	Low noise OpAmps II Low power OpAmps Low voltage Op Amps	Chapter 11 Chapter 1	402-414 393-402 415-432
16	4/24 4/26 4/28	360-370 390-400- 410	Comparators, two-stage open-loop comparators Discrete time, high speed comparators, autozeroing  Final exam preparation session		439-444 445-488
The <b>FINAL EXAM</b> is scheduled for Friday, May 5, 2006, from 2:50pm to 5:40pm					