Registers and Latches

Part A Implement a transparent latch using only four 2-input NAND gates and one inverter. Label *in*, *out*, and *enable* signals. Use correct mixed logic notation.

Part B Implement a **register with write enable**, using only transparent latches, NAND, NOR, AND, OR, and NOT gates. Use mixed logic design methodology. You do **not** have to implement transparent latches from basic gates. Label input and output signals $INPUT$, WE, $Phi1$, $Phi2$, and $OUTPUT$. Label the output of the first latch as X.

Part C Now complete the timing diagram for this register based on the specified inputs. Point X is defined as the output of the first latch in the register. OUT is the output of the register. Assume all internal storage is initially zero. Ignore gate propagation delay.