Combinational Design

Consider the expression: $Out = (\overline{A\,B} + \overline{C}\,D)\overline{(E + \overline{F})}$

Part A Use a mixed logic methodology to implement this expression using 2-input NOR gates and inverters. Do not simplify the expression. Do not assume the compliments of the signals are available. Determine how many transistors are required.

number of transistors = _____

Part B Repeat the previous part using only 2-input NAND gates and inverters.

number of transistors = _____

Part C Use DeMorgan's Theorem to eliminate all compliment bars in the expression except for those over single input variables ($\overline{A}, \overline{B}, etc.$). Write the new expression.

Out = _____

Part D Implement this new expression using transistor-level design. In this implementation, assume complimented inputs **are** available. How many transistors are required?

number of transistors = _____