

## Memory System Design

In the following sections, you will design three different memory systems using four memory chips. The chips used are **four million address** by **four bit words**.

**Part A** Consider a **four million address** by **sixteen bit word** memory system.

How many address lines does the memory system require? \_\_\_\_\_

How many data lines does the memory system require? \_\_\_\_\_

What kind of address decoder is required? \_\_\_\_\_ to \_\_\_\_\_

**Part B** Consider a **eight million address** by **eight bit word** memory system.

How many address lines does the memory system require? \_\_\_\_\_

How many data lines does the memory system require? \_\_\_\_\_

What kind of address decoder is required? \_\_\_\_\_ to \_\_\_\_\_

**Part C** Consider a **sixteen million address** by **four bit word** memory system.

How many address lines does the memory system require? \_\_\_\_\_

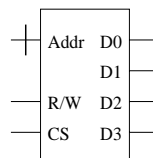
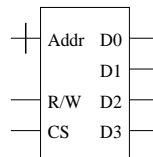
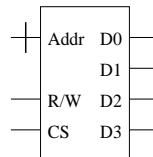
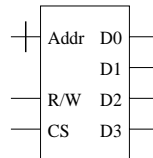
How many data lines does the memory system require? \_\_\_\_\_

What kind of address decoder is required? \_\_\_\_\_ to \_\_\_\_\_

**Part D** Now design each system below. Be sure you label the memory system inputs, Addr, R/W, and Mem Sel, and the system's outputs D0, D1, D2, etc. Also label bus widths, and inputs and outputs of any required decoders. **Put a star on the chips containing memory location 0.**

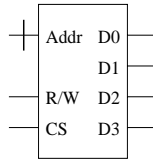
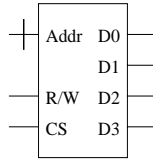
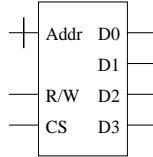
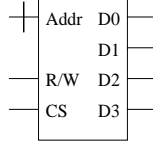
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4 million address  
16 bit words



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8 million address  
8 bit words



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16 million address  
4 bit words

