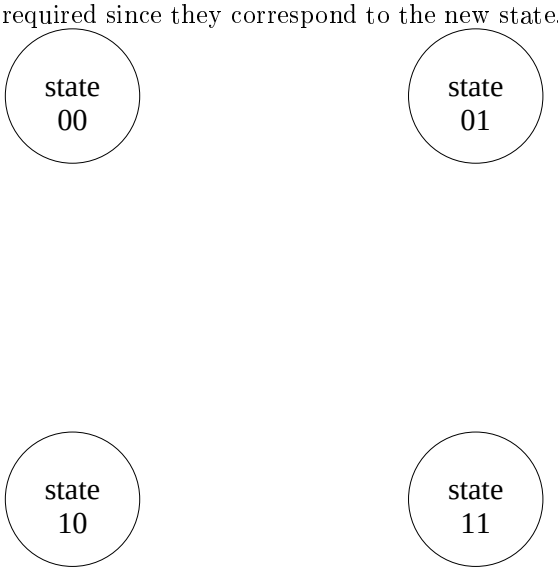
Up/Down State Machine

Consider a state machine implementation of a two bit up/down counter. The state machine has one input: $up/\overline{down}$, and two outputs: Out_0 and Out_1, which also indicate the next state. When $up/\overline{down}$ is high, the counter counts up (00,01,10,11,00, ...). When $up/\overline{down}$ is low, the counter counts down (00,11,10,01,00, ...).

Part A Complete the state diagram below by adding all required transition arcs with input annotations. Output annotations are not required since they correspond to the new state.



Part B Now complete the state table from the state diagram.

S_1	S_0	$up/\overline{down}$	O_1	O_0
0	0	0		
0	0	1		
0	1	0		
0	1	1		

S_1	S_0	$up/\overline{down}$	O_1	O_0
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Part C Derive a simplified expression for O_0 and O_1.

$O_0 =$ _____

$O_1 =$ _____

Part D Implement the up/down counter state machines using register cells for the state bits, plus basic gates.