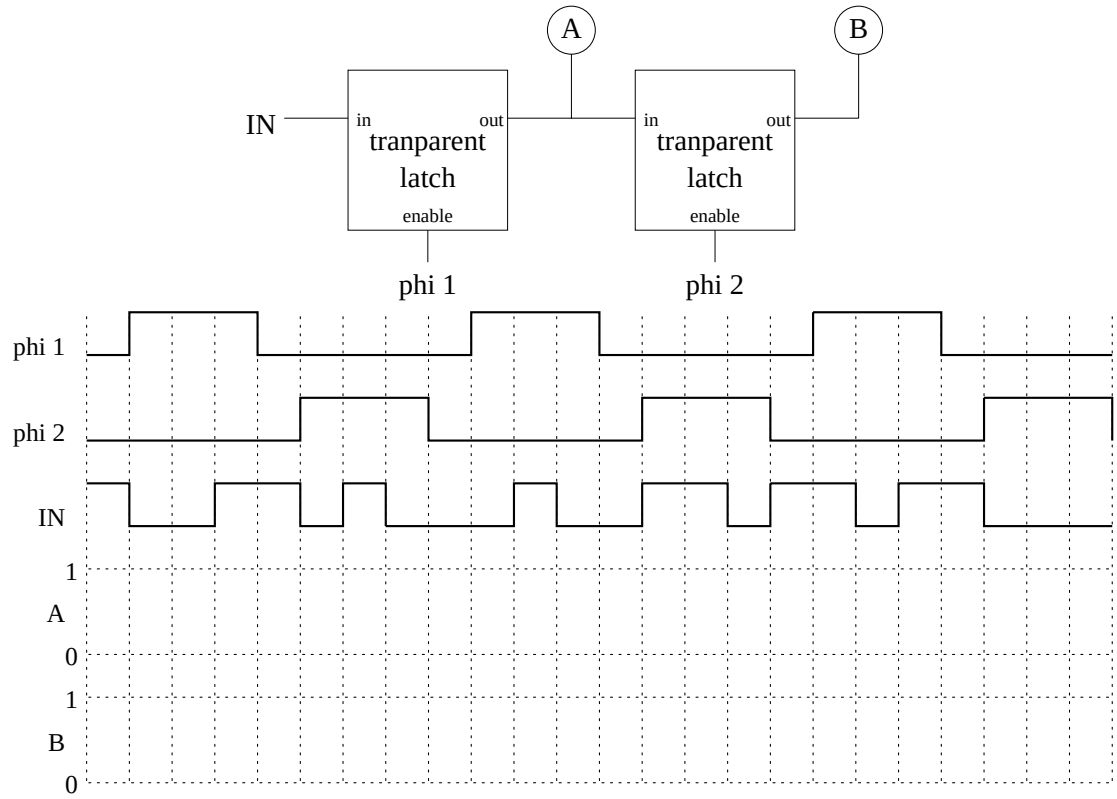
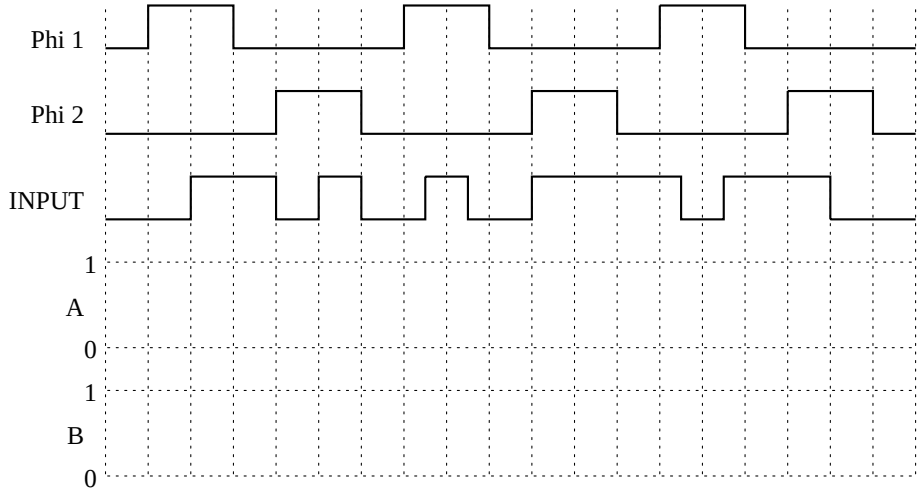
Registers

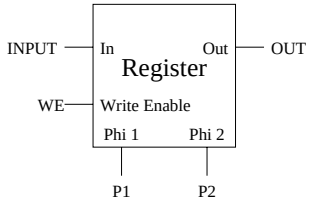
Part A Complete the timing diagram for the REGISTER shown below by determining test points A and B. Assume both latch states are initially zero.



Part B Complete the following timing diagram for the circuit above. Assume all latch values are initially zero.

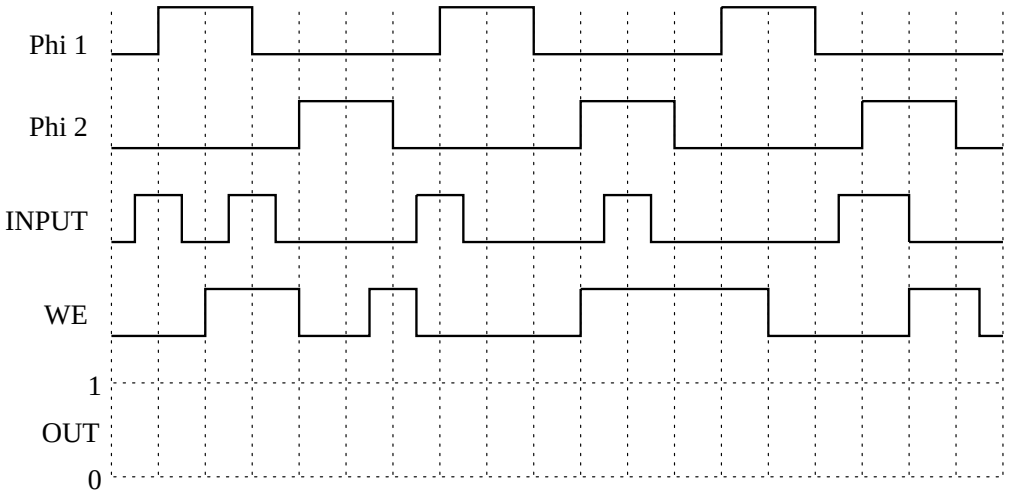


Part C Implement a **register with write enable** (shown below in icon form), using only transparent latches, NAND, NOR, AND, OR, and NOT gates. Use mixed logic design methodology. You do **not** have to implement transparent latches from basic gates.



Part D On the timing diagram below, draw a vertical line at each time where a new input value is sampled by the register. The new value should be different from the current value.

Part E Now complete the timing diagram for this register based on the specified inputs. Assume all internal storage is initially zero. Ignore gate propagation delay.



Part F On the timing diagram below, draw a vertical line at each time where a new input value is sampled by the register. The new value should be different from the current value.

Part G Now complete the timing diagram for this register based on the specified inputs. Assume all internal storage is initially zero. Ignore gate propagation delay.