Transparent Latches

Part A Complete the truth table to describe the circuit below:

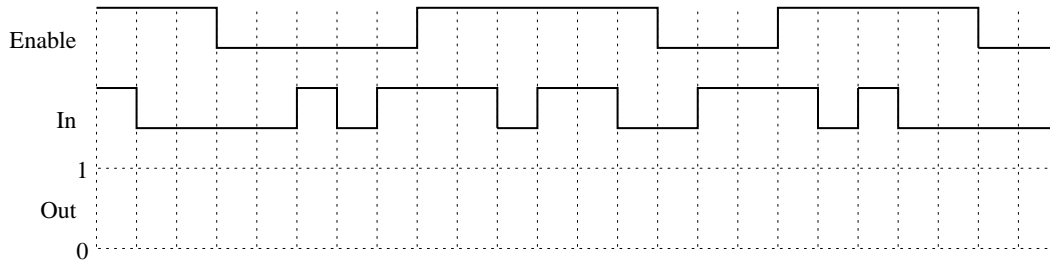| A B	Out
0 0	
1 0	
0 1	
1 1	
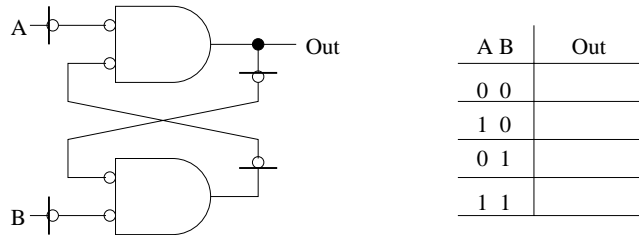
Part B Now consider a transparent latch based on this circuit (show below). How many transistors are used in this implementation?
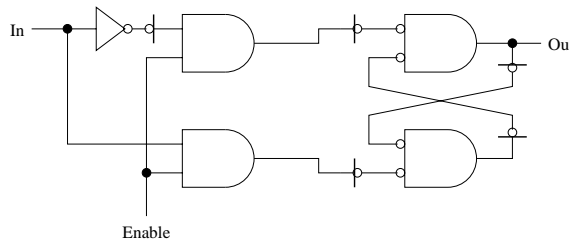
_____transistors

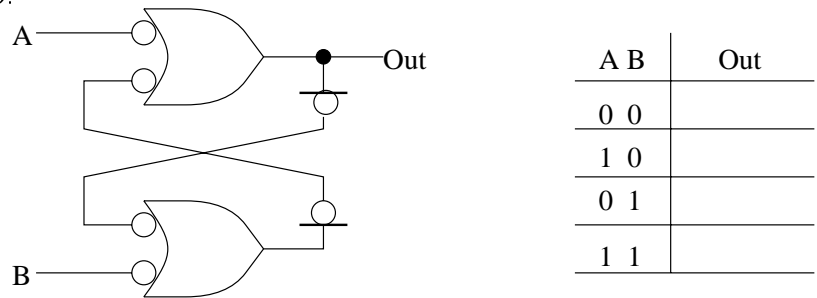**Part C** Complete the timing diagram for the latch output based on the specified inputs.

Part D Design a latch using four 2-input NOR gates and two inverters. Be sure to label the signals In, Out, and Enable.

Part E Design a transparent latch using four 2-input AND gates and five inverters. Be sure to label the signals In, Out, and Enable.

Part F Design a transparent latch using only four 2-input OR gates and six inverters. Be sure to label the signals In, Out, and Enable.

Part G Complete the truth table to describe the circuit below. Also indicate which states denote RESET, SET, and HOLD.

A B	Out
0 0	
1 0	
0 1	
1 1	

Part H Now consider a transparent latch based on this circuit (shown below). How many transistors are used in this implementation (show work)?
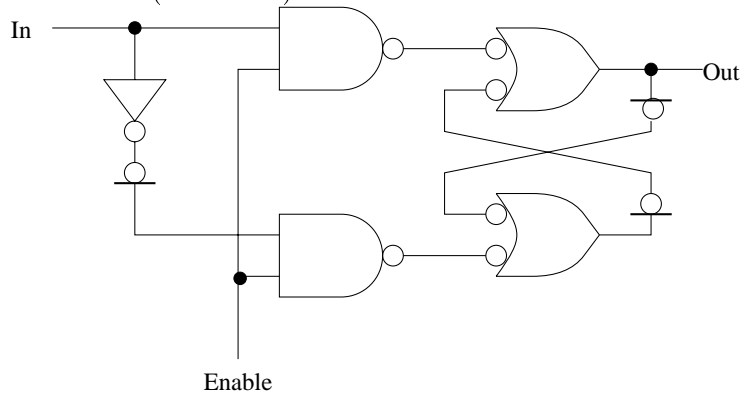
_____transistors

Part I Complete the timing diagram for the latch output based on the specified inputs.