**Instruction Format Solutions**

1. Suppose the an instruction set architecture has an immediate instruction format with the following fields and sizes:

| Opcode: 8 bits | Dest. Reg: 6 bits | Source 1 register: 6 bits | Immediate value: 20 bits |
|---|---|---|---|

What is the maximum number of opcodes? $2^{|OpcodeField|} = 256$

What is the number of registers? $2^{|RegisterField|} = 64$

What is the range of the signed immediate value? $\pm 2^{|ImmField|-1} = \pm 512K$

What is the instruction word size? 40 bits

2. Suppose a datapath has three operand busses (two source, one destination), 128 instruction types, and 64 registers where each register is 32 bits wide. Immediate operands can be in the range of ±64K. Determine the following values for the resulting instruction format. For the last two questions, assume the same operand number and types used in the MIPS format.

bits needed to specify an opcode 7

bits needed to specify a register operand 6

bits needed to specify an immediate operand 17

minimum bits needed to specify an R-format instruction 7+6+6+6=25

minimum bits needed to specify an I-format instruction 7+6+6+17=36

3. Suppose a datapath has three operand busses (two source, one destination), 45 instruction types, and 32 registers where each register is 16 bits wide. Immediate operands can be in the range of ±128K.

Design an instruction format for instructions that have one operation, one destination register and two source registers. Label the fields and minimum number of bits need for each field.

| Opcode: 6 | Dest. Register: 5 | Source1 Reg: 5 | Source2 Reg: 5 |
|---|---|---|---|

Design an instruction format for instructions that have one operation, one destination register, one source register, and an immediate value. Label the fields and minimum number of bits need for each field.

| Opcode: 6 | Dest. Register: 5 | Source1 Reg: 5 | Immediate: 18 |
|---|---|---|---|

4. Suppose we are designing an instruction set architecture with 32-bit instructions and 26 different opcodes. The register file contains 128 registers. One of the instruction types we would like to support specifies an opcode, a destination register, and two immediate source values. What is the minimum number of bits that are needed to specify each field?

| Opcode: 5 bits | Destination Register: 7 bits | Immediate value 1: 10 bits | Immediate value 2: 10 bits |
|---|---|---|---|

5. Suppose we are designing an instruction set architecture with 28-bit instructions and 44 different opcodes. Immediate operands can be in the range of ±512. How many registers can this

datapath have? Assume we would like to support an R-type and an I-type instruction format with the same operand number and types used in the MIPS format.

For I-type, the opcode and immediate fields must be 6 bits and 10 bits, respectively.

| Opcode: 6 | Dest. Register: ? | Source1 Reg: ? | Immediate: 10 |
|---|---|---|---|

If the overall instruction length is 28 bits, that leaves 12 bits for the two register fields. So there are 6 bits per register field, enough to specify one of **64 registers**.

For R-type, 6 bits per register and a 6-bit opcode field takes 24 bits, which is within the 28-bit instruction length.

| Opcode: 6 | Dest. Register: ? | Source1 Reg: ? | Source2 Reg: ? |
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