

*This exam will be conducted according to the Georgia Tech Honor Code. I pledge to neither give nor receive unauthorized assistance on this exam and to abide by all provisions of the Honor Code.*

**Signed (With your Full Legal Name):**

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*Instructions:* Instructions: This is a closed book, closed note exam. Calculators are not permitted. If you have a question, raise your hand and I will come to you. Please work the exam in pencil and do not separate the pages of the exam. For maximum credit, show your work.

Good Luck!

Your Name (please print): \_\_\_\_\_

For maximum (and partial) credit, show your work.

*Good Luck!*

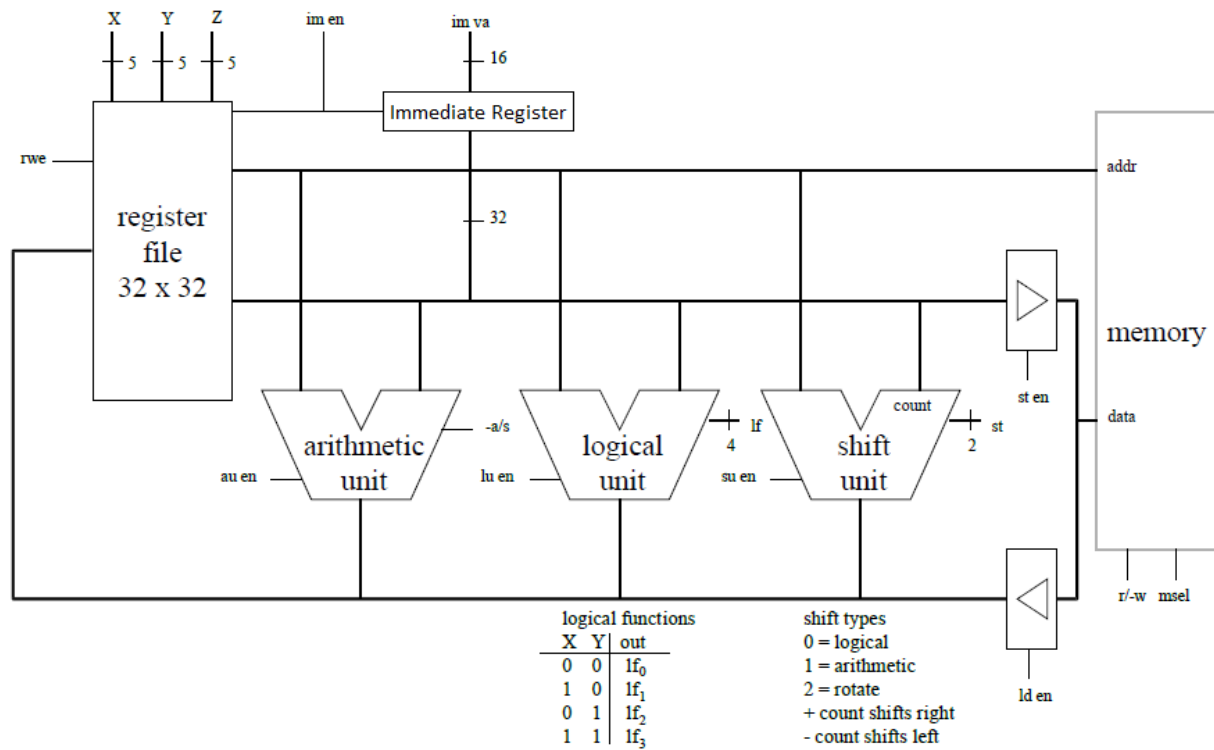
1	2	3	4	5	total
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12	18	30	20	20	100

## Datapath Signals and Diagram

Cycle	Cycle number
X	Register driven onto X bus
Y	Register driven onto Y bus
Z	Register written from Z bus
rwe	Register write enable
im_en	Immediate enable on Y bus
im_va	Immediate value
au_en	Arithmetic unit enable
$\bar{a}/s$	Register driven onto X bus

lu_en	Logical unit enable
lf	Logical function
su_en	Shift unit enable
st	Shift type
ld_en	Load enable
st_en	Store enable
r/ $\bar{w}$	Read/write (0 = write, 1 = read)
mselect	Memory select
description	Operation description

Logical Function Examples			
X	Y	X and Y (LF = 8)	X+Y (LF = E)
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1



Problem 1 (4 parts, 12 points)

Fundamentals

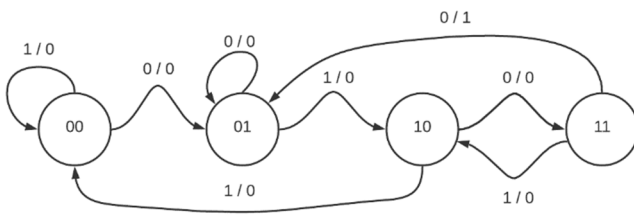
Part A (4 points) Suppose the following inputs (in hexadecimal, denoted by 0x) are applied to an 8-bit shifter. Determine the output (in hexadecimal).

Shift Type	Shift Amount	Input Value	Output Value
arithmetic	0xFE	0x52	<b>0x48</b>
rotate	0x05	0x14	<b>0xA0</b>

Part B (2 points) Flip/flops are different from latches in that the output changes constantly if the control signal is asserted.

- a) True
- b) False

Part C (4 points) Identify whether the following systems are Moore or Mealy machines.



S	EN	S*	Z
A	0	D	1
A	1	B	1
B	0	A	0
B	1	B	0
C	0	C	1
C	1	A	1
D	0	B	1
D	1	D	1

a) Moore

b) Mealy

a) Moore

b) Mealy

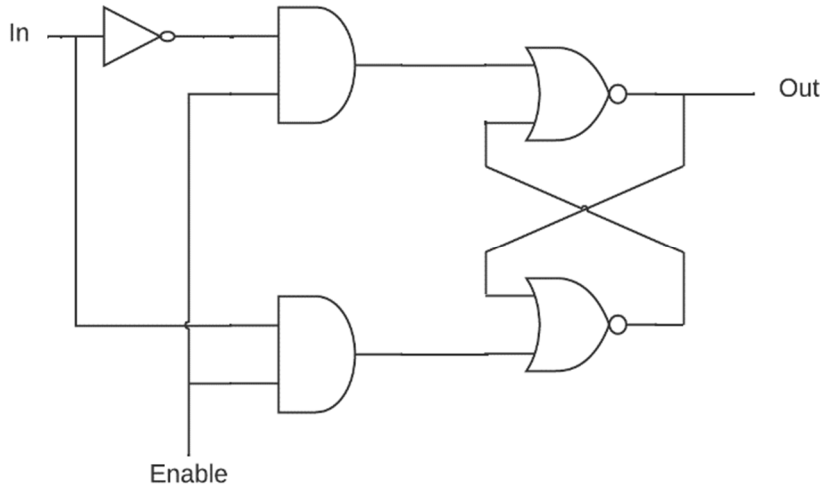
Part D (2 points) Which of the following functional units is a sequential element that controls the timing for the overall datapath?

- a) Logic Unit
- b) X Bus
- c) Register File
- d) Memory Select signal

Problem 2 (2 parts, 18 points)

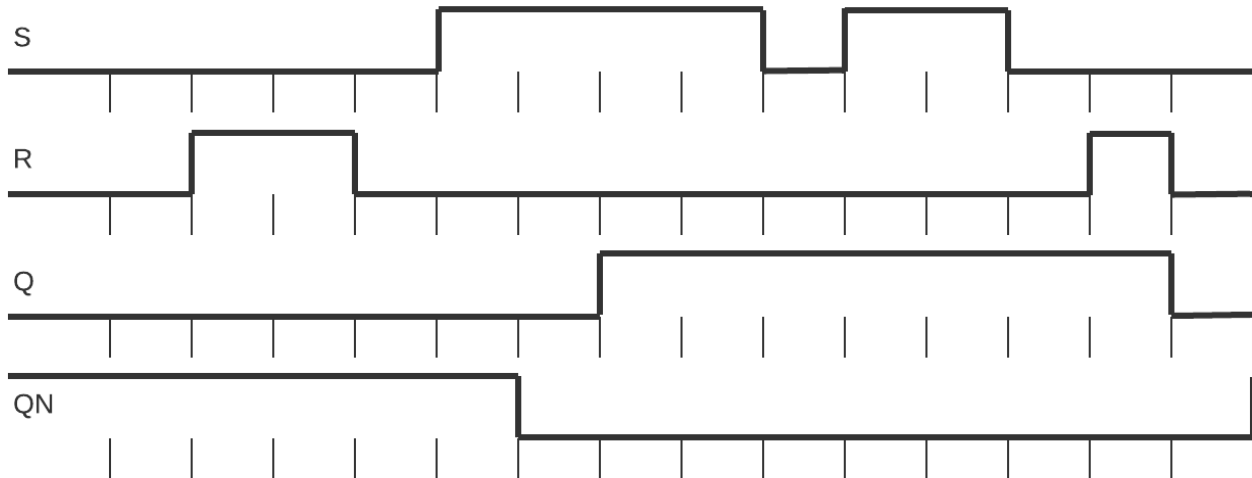
Latches and Flip/Flops

Part A (8 points) For the circuit below, complete the truth table describing its behavior.



In	Enable	Out
0	0	$Q_0$
0	1	0
1	0	$Q_0$
1	1	1

PART B (10 points) Predict the expected output (Q and QN) for an SR latch given the input waveforms shown below. Assume that there is a 10 ns delay for each gate and that the time scale is 10 ns per division. Assume that the latch is initially stable in the Reset state.



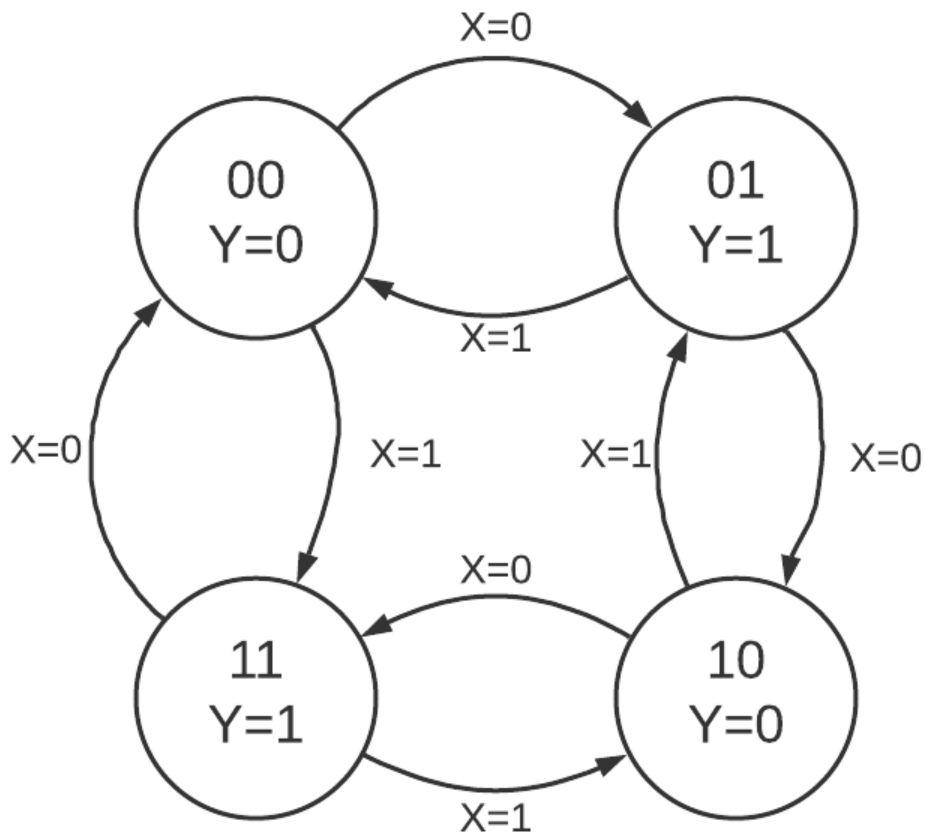
Problem 3 (3 parts, 30 points)

Finite State Machines

Consider the following excitation table for a finite state machine with X as the input and Y as the output.

Q2	Q1	X	Q2*	Q1*	Y
0	0	0	0	1	0
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	1	0	1

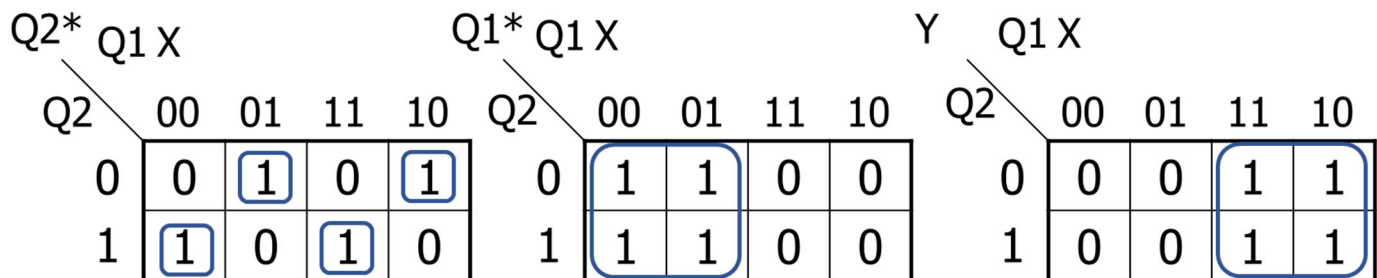
PART A (10 points) Draw its finite state machine diagram using the circles below. Label all states, inputs, and outputs.



Consider the following excitation table for a finite state machine with X as the input and Y as the output.

Q2	Q1	X	Q2*	Q1*	Y
0	0	0	0	1	0
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	1	0	1

PART B (10 points) Derive the simplified excitation and output equations needed to build the sequential circuit diagram for this finite state machine.



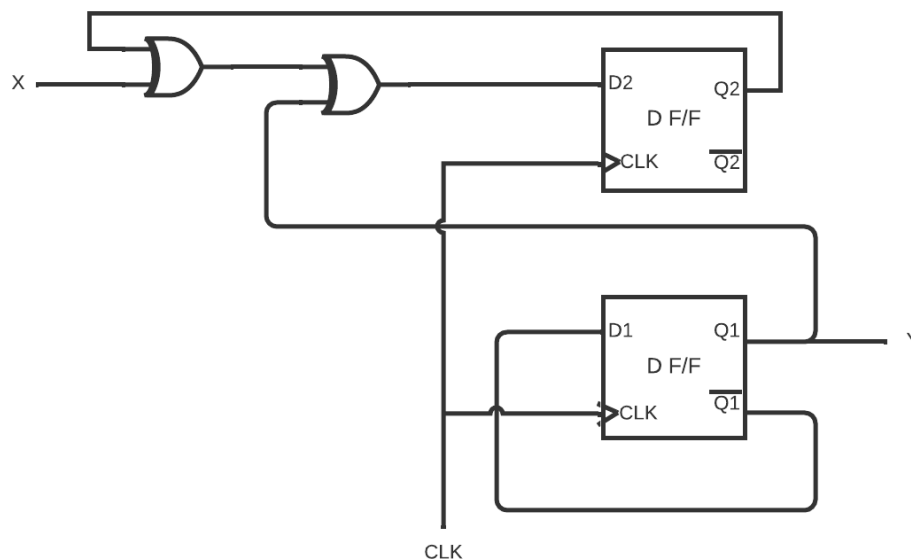
$$Q2^* = Q2\overline{Q1}\overline{X} + \overline{Q2}Q1X + Q2Q1X + \overline{Q2}Q1\overline{X}$$

$$= Q2 \oplus (Q1 \oplus X)$$

$$Q1^* = \overline{Q1}$$

$$Y = Q1$$

PART E (10 points) Draw the sequential circuit diagram for the state machine using the building blocks below and any basic gates (AND, OR, NAND, NOR, XOR, NOT) you require. Assume clock inputs to the flip/flops (and any other control signals) are already connected.



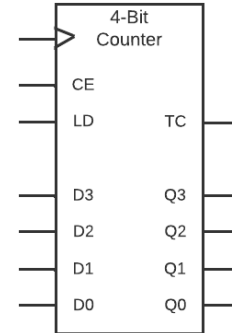
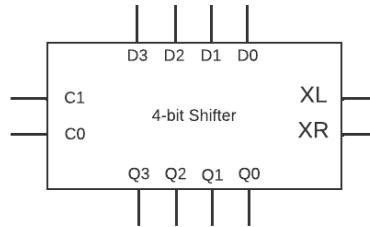
Problem 4 (2 parts, 20 points)

Finite State Machines

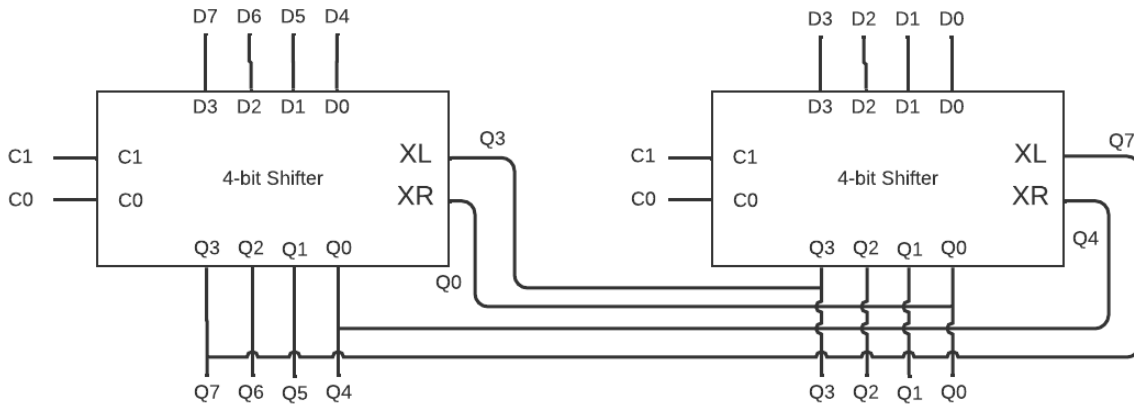
Consider the following sequential building blocks.

Shifter Control Signals

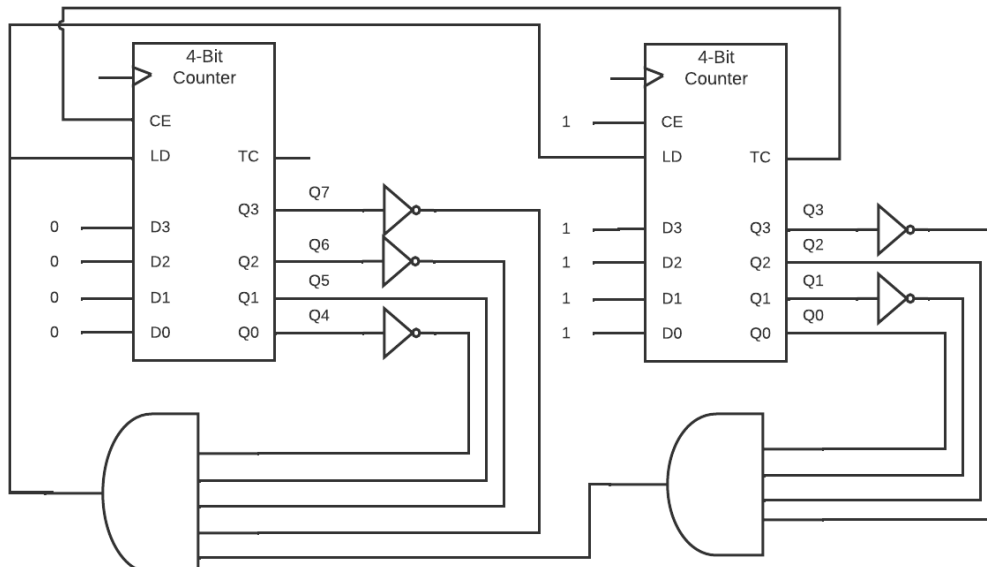
C1	C0	Behavior
0	0	No shift
0	1	Shift left
1	0	Shift right
1	1	Parallel load



PART A (10 points) Design an 8-bit rotate register (without carry) using the 4-bit bidirectional shifters above.



PART B (10 points) Design a binary counter that counts from 15 to 37 using the 4-bit counter with parallel load above. Assume that the counter begins operation based on the load signal.



Problem 5 (3 parts, 20 points)

Microcode

Using the datapath on Page 2, write microcode fragments for the following procedures. Express all values in hexadecimal notation. Use 'x' when a value does not matter. For maximum credit, complete the description field to describe the sub-operation for each row. In each part, modify only registers 3 and 6.

PART A (4 points)

$$R_3 = (R_6 \text{ or } R_1) \text{ and } R_2$$

#	X	Y	Z	rwe	im en	im va	au en	a/s	lu en	LF	su en	ST	st en	ld en	r/w	msel	Description
1	6	1	3	1	0	X	0	X	1	E	0	X	0	0	X	X	R3 = R6 or R1
2	3	2	6	1	0	X	0	X	1	8	0	X	0	0	X	X	R3 = R3 and R2
3																	

PART B (8 points)

$$R_3 = \frac{R_4}{4} + R_7$$

#	X	Y	Z	rwe	im en	im va	au en	a/s	lu en	LF	su en	ST	st en	ld en	r/w	msel	Description
1	4	X	3	1	1	2	0	X	0	X	1	1	0	0	X	X	R3 = R4 \ 4
2	3	7	3	1	0	X	1	0	0	X	0	X	0	0	X	X	R3 = R3 + R7
3																	
4																	

PART C (8 points)

$$M[R_6] = (R_4 + R_3) - 7$$

#	X	Y	Z	rwe	im en	im va	au en	a/s	lu en	LF	su en	ST	st en	ld en	r/w	msel	Description
1	3	4	3	1	0	X	1	0	0	X	0	X	0	0	X	X	R3 = R4 + R3
2	3	X	3	1	1	7	1	1	0	X	0	X	0	0	X	X	R3 = R3 - 7
3	6	3	X	1	0	X	0	X	0	X	0	X	1	0	0	1	M[R6] = R3
4																	