Problem 1 (3 parts, 31 points) Numbers of Reason

Part A (13 points) Convert the following notations:

binary notation	decimal notation
1 1100 1001.1001	457.5625
1 1111 0001	497
1 1001.11	25.75
binary notation	**hexadecimal notation**
101 1010 0101.0101 1010 101	5A5.5AA
1100 1010 0001 0001.1100 1010 1011	CA11.CAB

Part B (12 points) For the 25 bit representations below, determine the most positive value and the step size (difference between sequential values). **All answers should be expressed in decimal notation**. Fractions (e.g., 3/16ths) may be used. Signed representations are two's complement.

representation	most positive value	step size
unsigned fixed-point (20 bits) . (5 bits)	1M	1/32
signed integer (25 bits) . (0 bits)	16M	1
signed fixed-point (13 bits) . (12 bits)	4K	1/4K
signed fixed-point (9 bits) . (16 bits)	256	1/64K

Part C (6 points) A 25 bit floating point representation has a 17 bit mantissa field, a 7 bit exponent field, and one sign bit.

What is the largest value that can be represented (closest to infinity)? 2^{63}

What is the smallest value that can be represented (closest to zero)? 2^{-64}

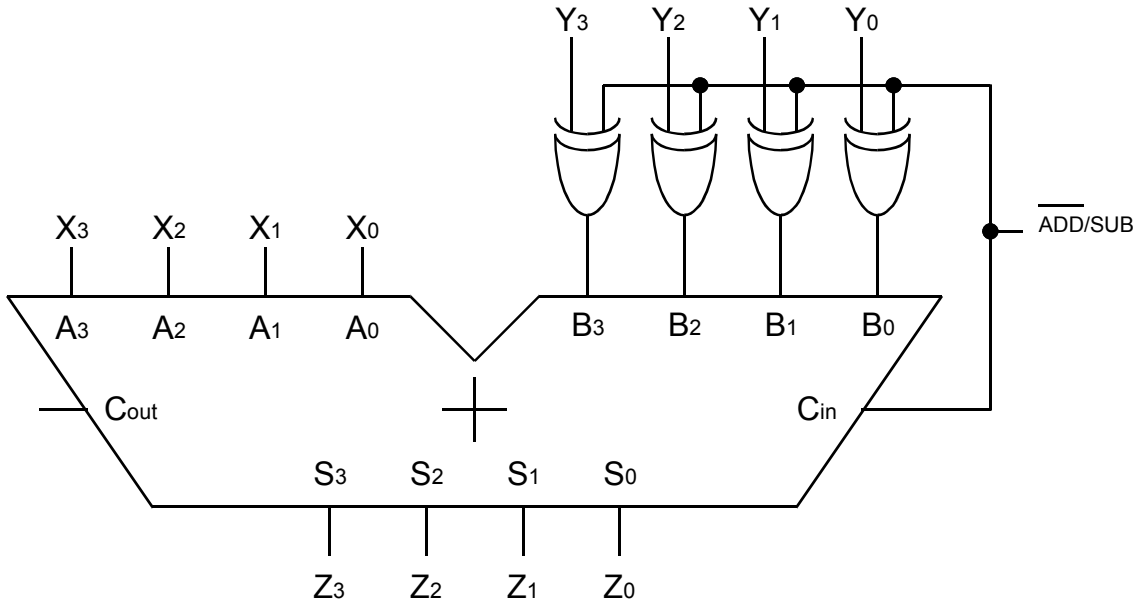
How many decimal significant figures are supported? 5

Problem 2 (3 parts, 24 points) "It doesn't add up"

Part A (12 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a **five bit unsigned fixed-point** and **five bit two's complement fixed-point** representations.

	11.1 + 111.1	1101.1 + 1100.1	0.0 -1000.1	1010.1 - 101.0
result	1011.0	1010.0	0111.1	101.1
unsigned error?	■ no □ yes	□ no ■ yes	□ no ■ yes	■ no □ yes
signed error?	□ no ■ yes	■ no □ yes	■ no □ yes	□ no ■ yes

Part B (6 points) The adder below adds two four bit numbers A and B and produces a four bit result S. Add extra digital logic to support subtraction as well as addition. Label inputs X_3, X_2, X_1, X_0, Y_3, Y_2, Y_1, Y_0, $\overline{ADD}/SUB$ and outputs Z_3, Z_2, Z_1, Z_0.



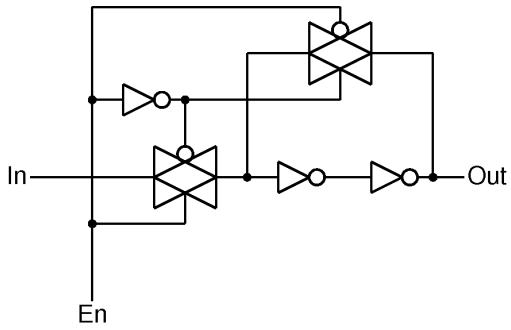
Part C (6 points) Write two Boolean expressions indicating signed two's complement addition and subtraction overflow using inputs X_3, Y_3, Z_3. These SOP expressions should be true when overflow occurs.

addition overflow = $X_3\, Y_3\, \overline{Z}_3 + \overline{X}_3\, \overline{Y}_3\, Z_3$

subtraction overflow = $X_3\, \overline{Y}_3\, \overline{Z}_3 + \overline{X}_3\, Y_3\, Z_3$

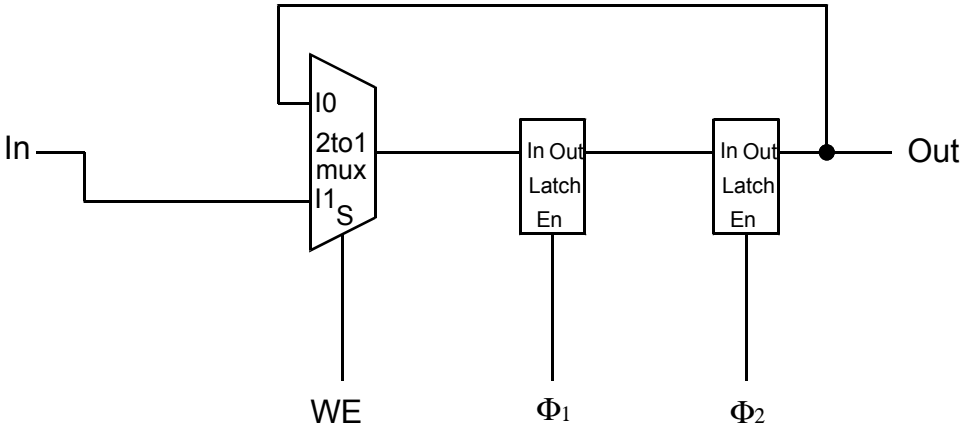
Problem 3 (3 parts, 24 points) Achieve a Happy State

Part A (10 points) Implement a transparent latch using **only pass gates and inverters**.



IN	EN	OUT	$\overline{OUT}$
A	0	Q_0	$\overline{Q}_0$
A	1	A	$\overline{A}$

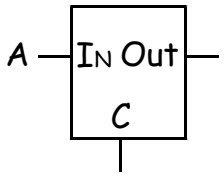
Part B (8 points) Implement a one bit register with write enable using only the components drawn below. Label inputs **In**, *write enable* **WE**, clocks ϕ_1, and ϕ_2, and output **Out**.



Part C (6 points) Assume the following signals are applied to a register. Draw the output signal **Out**. Draw a vertical line where **In** is sampled. *Draw crosshatch where **Out** is unknown.*

Problem 4 (3 parts, 21 points) "A chip off the old block"

Part A (15 points) Consider the five definitions for the block drawn below. One block input is the logical value **A**. The other input is the control value **C**. The output behavior for each of the five definitions is given in the table. Complete the full truth table and state the *logical (gate) names* for each definition. (hint: the first block one appears to mask **A** when its control input is low.)



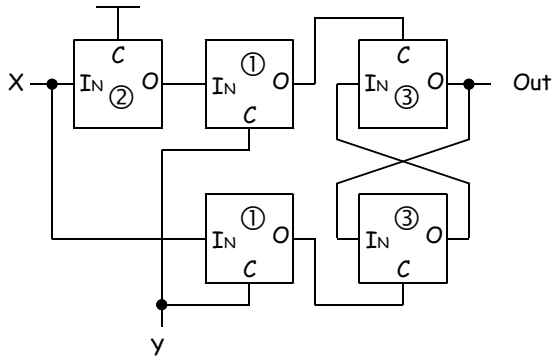
In	C	①	②	③	④	⑤
A	0	0	A	$\overline{A}$	A	Z_o
A	1	A	$\overline{A}$	0	1	A

In	C	①	②	③	④	⑤
0	0	0	0	1	0	Z_o
1	0	0	1	0	1	Z_o
0	1	0	1	0	1	0
1	1	1	0	0	1	1

① AND ② XOR ③ NOR

④ OR ⑤ Pass Gate

Part B (6 points) The circuit below is built using these blocks. Describe its behavior. Also give the circuits common name.



X	Y	Out
0	0	Q_0
1	0	Q_0
0	1	0
1	1	1

It's a transparent latch