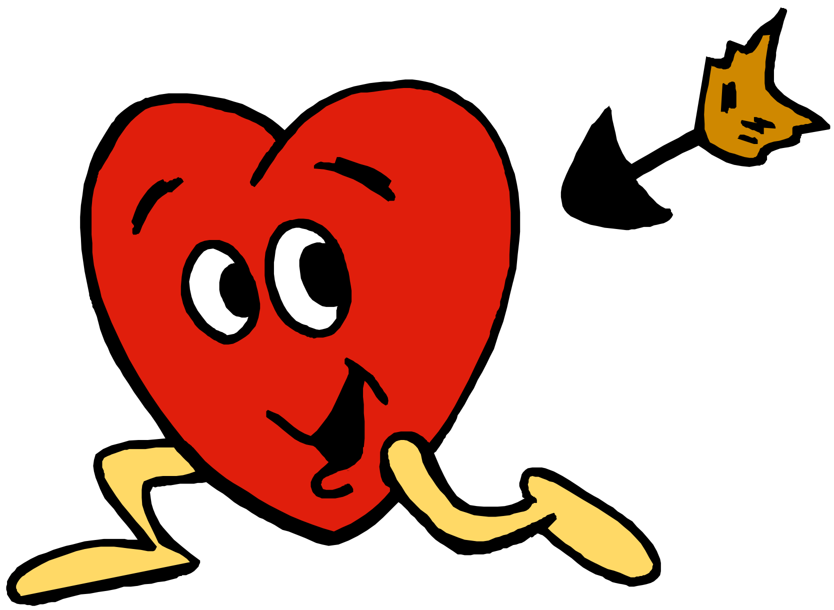
Instructions: This is a closed book, closed note exam. Calculators are not permitted. If you have a question, raise your hand and I will come to you. Please work the exam in pencil and do not separate the pages of the exam. For maximum credit, show your work.
Good Luck!

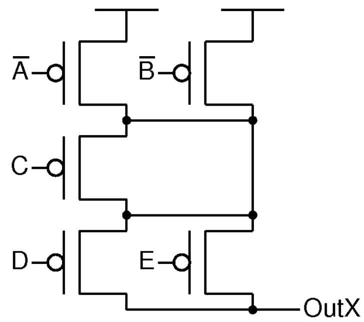
Your Name (***please print***) ____

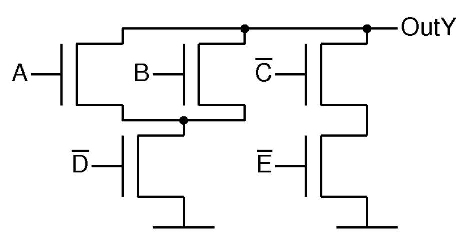
1	2	3	4		total
30	20	26	24		100



Problem 1 (3 parts, 30 points) Incomplete Circuits

The three parts below contain (A) a pull up network, (B) a pull down network, and (C) an expression to be implemented. For (A) and (B), complete the missing complementary switching networks so the circuit contains no floats or shorts and write the Boolean expression computed by the completed circuit. For (C), design the entire switching network. Assume the inputs and their complements are available.





OutX =

OutY =

OutZ = $(A + B \cdot \overline{C} + D) \cdot \overline{E}$

Problem 2 (2 parts, 20 points) — Boolean Algebra

Part A (12 points) Transform each of the following Boolean expressions to a equivalent form where *they contain only AND operations*. **Do not implement**.

$$OUT_X = \overline{\overline{A} \cdot B + C \cdot \overline{D}}$$ ____________________________________

$$OUT_Y = \overline{\overline{A} \cdot \overline{B + C} \cdot \overline{D + E}}$$ ____________________________________

Part B (8 points) Derive the canonical product of sums (using maxterms) expression using the behavior expressed in the truth table.

A	B	C	$F_{(A,B,C)}$
0	0	0	0
1	0	0	1
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

$POS_{(MAXTERMS)} =$ ____

Problem 3 (2 parts, 26 points) Mixed Logic Design

Part A (10 points) Implement a two-input odd parity gate (XOR) using basic gates and inverters to minimize implementation cost. Use proper mixed logic notation. Assume only true inputs (X and Y) are available. Tally the implementation transistors. Hint: $Out = X \cdot \overline{Y} + \overline{X} \cdot Y$

transistors = ______________________

Part B (16 points) Implement the follow expression using basic gates and inverters to minimize implementation cost. Use proper mixed logic notation. Assume only true inputs are available. *Do not modify the expressions being implemented*. Show the implementation cost (in transistors).

$$OUT_X = \overline{A} \cdot B + \overline{(C + \overline{D} + E)}$$

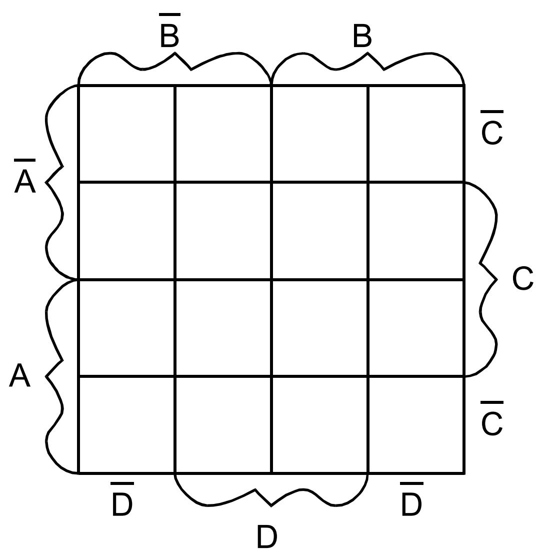
$$OUT_Y = (C + \overline{D} + E) \cdot (\overline{F} + G)$$

transistors = ______________________

Problem 4 (2 parts, 24 points) Karnaugh Maps

Part A (12 points) For the follow expression, derive a simplified ***sum of products*** expression using a Karnaugh Map. Circle and list *all* prime implicants, indicating which are essential.

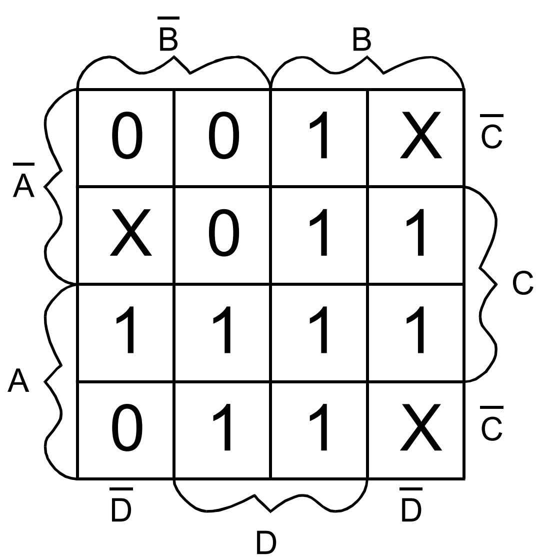
$$Out = (A+C+D)\cdot(B+C+D)\cdot(\overline{A}+B+\overline{D})\cdot(\overline{A}+\overline{B}+\overline{C}+\overline{D})$$



prime implicants	essential? yes	no
________________	☐	☐
________________	☐	☐
________________	☐	☐
________________	☐	☐
________________	☐	☐
________________	☐	☐
________________	☐	☐
________________	☐	☐

simplified **SOP** expression ________________________________

Part B (12 points) For the behavior in the map below, derive a simplified ***product of sums*** expression. Circle and list all prime implicants, indicating which are essential.



prime implicants	essential? yes	no
________________	☐	☐
________________	☐	☐
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simplified POS expression ________________________________