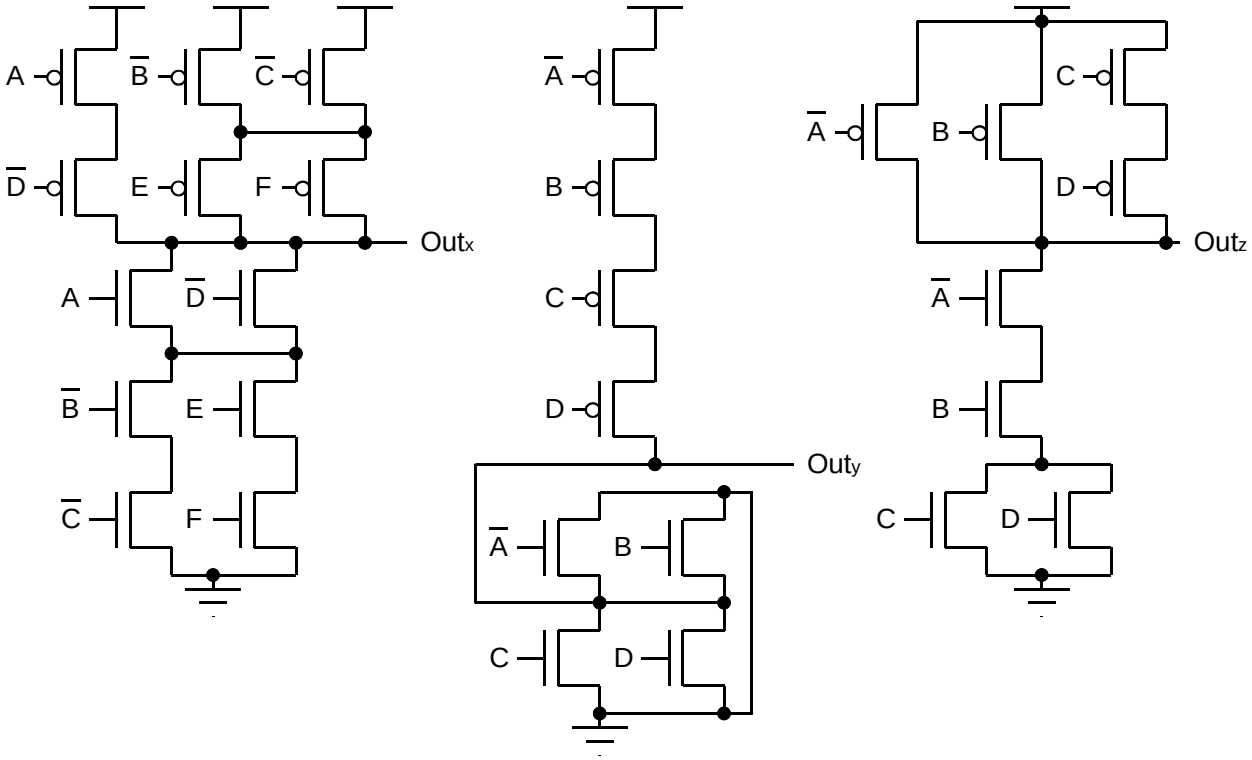
Problem 1 (3 parts, 30 points) Incomplete Circuits

The three parts below contain (A) a pull up network, (B) a pull down network, and (C) an expression to be implemented. For (A) and (B), complete the missing complementary switching networks so the circuit contains no floats or short and write the Boolean expression computed by the completed circuit. For (C), design the entire switching network. Assume the inputs and their complements are available.



OUTx = $\overline{A} \cdot D + (B + C) \cdot (\overline{E} + \overline{F})$

OUTy = $A \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$

OUTz = $A + \overline{B} + \overline{C} \cdot \overline{D}$

Problem 2 (2 parts, 20 points) Boolean Algebra

Part A (12 points) Transform each of the following Boolean expressions to a form where they are ready for switch level implementation (i.e., there should only be bars over input variables, not over operations). The behavior of the expression should remain unchanged. **Do not implement**.

$$OUT_X = \overline{\overline{\overline{A}\cdot B} + \overline{C}\cdot\left(D+\overline{E}\right)} \qquad = \overline{A}\cdot B\cdot\overline{\overline{C}\cdot\left(\overline{D+\overline{E}}\right)} = \overline{A}\cdot B\cdot\left(C+\overline{D+\overline{E}}\right) = \overline{A}\cdot B\cdot\left(C+\overline{D}\cdot E\right)$$

$$OUT_Y = \overline{A\cdot B\cdot\overline{C\cdot\overline{D}}} \qquad = \overline{A}+B\cdot\overline{C\cdot\overline{D}} = \overline{A}+B\cdot\left(\overline{C}+D\right)$$

Part B (8 points) Derive a canonical sum of products (using minterms) and a product of sums (using maxterms) expression for the truth table below.

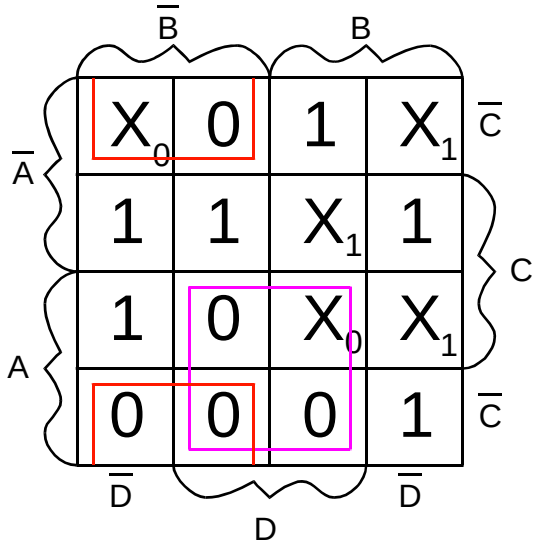
A	B	C	$F_{(A,B,C)}$
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	1

$SOP_{(MINTERMS)}$ = $\overline{A}\cdot B\cdot\overline{C} + \overline{A}\cdot\overline{B}\cdot C + A\cdot\overline{B}\cdot C + A\cdot B\cdot C$

$POS_{(MAXTERMS)}$ = $\left(A+B+C\right)\cdot\left(\overline{A}+B+C\right)\cdot\left(\overline{A}+\overline{B}+C\right)\cdot\left(A+\overline{B}+\overline{C}\right)$

Problem 3 (3 parts, 28 points) Karnaugh Maps

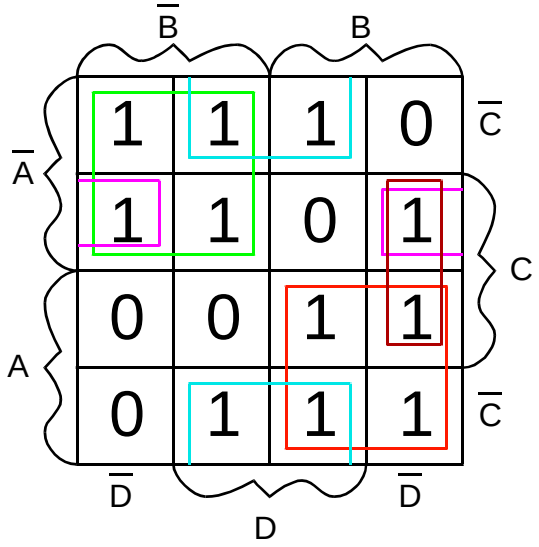
Part A (8 points) Using the following Karnaugh map definition of a behavior, specify each don't care and identify prime implicants for a simplified ***product of sums*** expression. List all PIs.



prime implicants	essential? yes	no
$\overline{A} + \overline{D}$	☒	☐
$B + C$	☒	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐

simplified **POS** expression $(\overline{A}+\overline{D})\cdot(B+C)$

Part B (8 points) For the follow behavior (expressed in map form), derive a simplified ***sum of products*** expression using a Karnaugh Map. Circle and list all prime implicants, indicating which are essential.

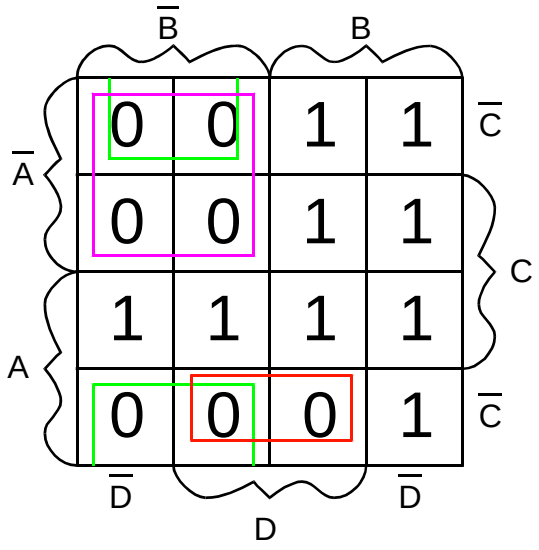


prime implicants	essential? yes	no
$\overline{A} \cdot \overline{B}$	☒	☐
$A \cdot B$	☒	☐
$\overline{C} \cdot D$	☒	☐
$B \cdot C \cdot \overline{D}$	☐	☒
$\overline{A} \cdot C \cdot \overline{D}$	☐	☒
	☐	☐
	☐	☐
	☐	☐

simplified SOP expression $\overline{A}\cdot\overline{B}+\overline{C}\cdot D+A\cdot B+B\cdot C\cdot\overline{D} = \overline{A}\cdot\overline{B}+\overline{C}\cdot D+A\cdot B+\overline{A}\cdot C\cdot\overline{D}$

Part C (12 points) For the follow expression, derive a simplified ***product of sums*** expression using a Karnaugh Map. Circle and list all prime implicants, indicating which are essential.

$$Out = (A + B + \overline{C}) \cdot (B + C + D) \cdot (\overline{A} + C + \overline{D}) \cdot (B + C + \overline{D})$$



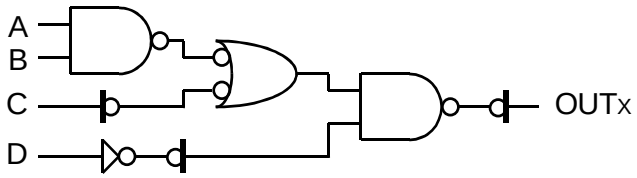
prime implicants	essential? yes	no
A + B	☒	☐
B + C	☒	☐
$\overline{A}$ + C+ $\overline{D}$	☒	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐

simplified POS expression $(A+B)\cdot(B+C)\cdot(\overline{A}+C+\overline{D})$

Problem 4 (2 parts, 22 points) Mixed Logic Design

Part A (10 points) Implement the following expression using multi-input **NAND** gates and inverters. Minimize the total transistors (switches) required. Use proper mixed logic design technique. Do not simplify the expression.

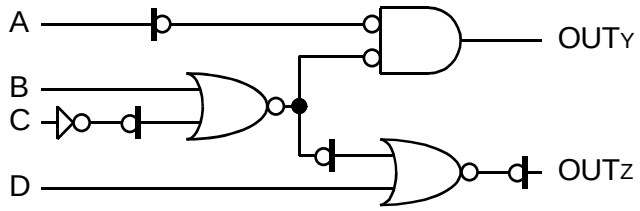
$$OUT_X = \overline{(A \cdot B + \overline{C}) \cdot \overline{D}}$$



transistors = 3 x 4t + 1 x 2t = 14t

Part B (12 points) Implement the following two expressions using multi-input **NOR** gates and inverters. Minimize the total transistors (switches) required. Use proper mixed logic design technique. Do not simplify the expressions.

$$OUT_Y = \overline{A} \cdot \left(B + \overline{C} \right) \qquad OUT_Z = \overline{\overline{B + \overline{C} + D}}$$



transistors = 3 x 4† + 1 x 2† = 14†