Problem 1 (3 parts, 30 points) Memory Systems

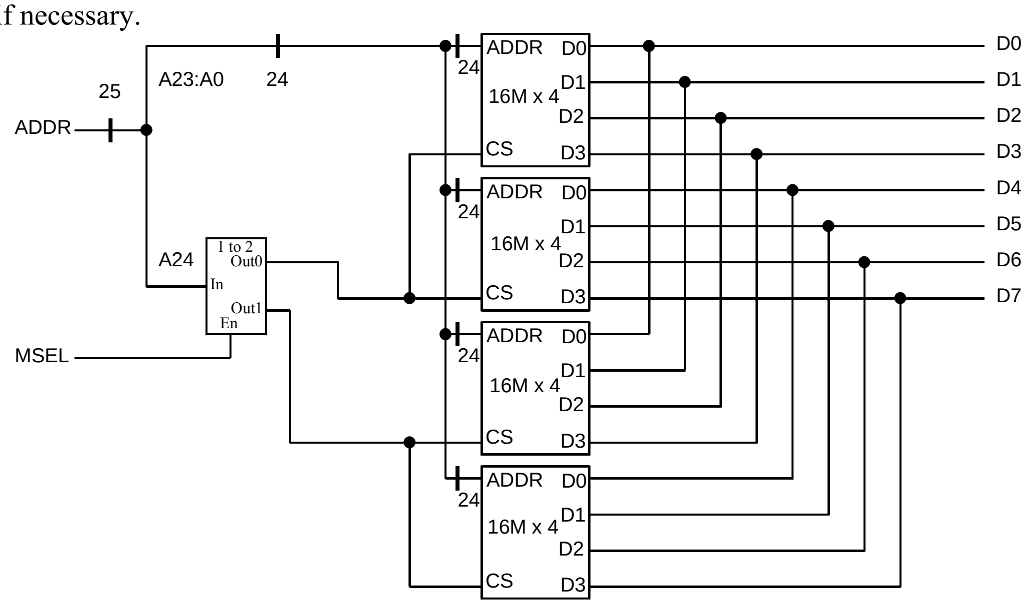
Part A (12 points) Consider a DRAM chip organized as **4 million addresses** of **64-bit words**. Assume both the DRAM cell and the DRAM chip are square. The column number and offset concatenate to form the memory address. Using the organization approach discussed in class, answer the following questions about the chip. *Express all answers in decimal (not powers of two).*

number of columns	$4M \times 64 = 2^{22} \times 2^6 = 2^{28}$; $2^{14} = 16K$
number of words per column	$2^{14}/2^6 = 2^8 = 256$
column decoder required (*n* to *m*)	14 to 16K
total number of bits in address	$\log_2(4M) = 22$
type of mux required (*n* to *m*)	256 to 1
number of address lines in column offset	8

Part B (10 points) Consider a memory system with **16 million addresses** of **32-bit words** using a **2 million** address by **8-bit word** memory DRAM chip.

word address lines for memory system	$\log_2(16M) = 24$
chips needed in one bank	32/8 = 4
banks for memory system	16M / 2M = 8
memory decoder required (*n* to *m*)	3 to 8
DRAM chips required	4 x 8 = 32

Part C (8 points) Design a 32 million address by 8 bit memory system with four 16M x 4 memory chips. *Label all busses and indicate bit width.* Assume R/W is connected and not shown here. Use a bank decoder if necessary.



Problem 2 (3 parts, 24 points) Datapath Elements

Part A (6 points) Suppose the following inputs (in `hexadecimal`) are applied to the 32-bit barrel shifter used in the datapath. Determine the output (in `hexadecimal`). Assume the shift amount is drawn from the 16-bit immediate value.

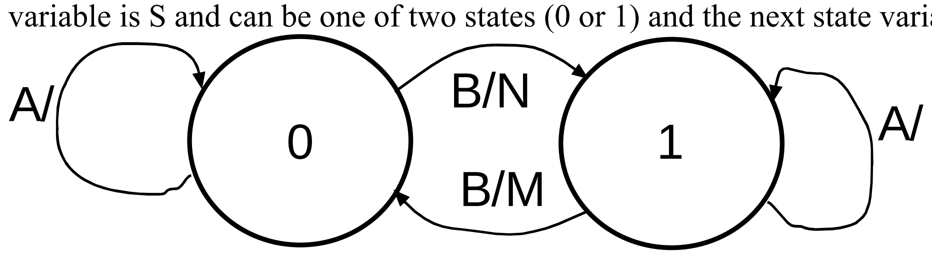
Shift Type	Shift Amount	Input Value	Output Value
logical	0xFFF4	EB25ACE7	5ACE7000
arithmetic	0x0008	CAB15317	FFCAB153
rotate	0x000C	DE2F1B36	B36DE2F1

Part B (8 points) For each bitwise logical function specification below, determine the LF code (in hexadecimal) to correctly program the logical unit.

X Y	Out
0 0	LF_0
1 0	LF_1
0 1	LF_2
1 1	LF_3

logical function	LF
$\overline{Y}$	3
$Y \cdot \overline{X}$	4
$X + \overline{Y}$	B
$X \cdot Y$	8

Part C (10 points) Given the following finite state diagram, fill in the state table below. The current state variable is S and can be one of two states (0 or 1) and the next state variable is NS.



S	$A/\overline{B}$	NS	M	N
0	0	1	0	1
0	1	0	0	0
1	0	0	1	0
1	1	1	0	0

Give the Boolean expression for computing NS in terms of the current state and the input.

NS = $\overline{S \oplus A}$ or $\overline{S} \cdot B + S \cdot A$

Problem 3 (3 parts, 26 points) Microcode

Using the supplied datapath, write microcode fragments to accomplish the following procedures. Express all values, except memory addresses, in hexadecimal notation. Use 'X' when a value is don't cared. For maximum credit, complete the description field. $\oplus$ means bitwise logical XOR.
In each part, modify only registers 7 & 8.

Part A (6 points) $R_7 = 15 \cdot R_8$

#	X	Y	Z	rwe	im en	im va	au en	-a /s	lu en	lf	su en	st	ld en	st en	r/ -w	msel	description
1	8	X	7	1	1	FFFC	0	X	0	X	1	1	0	0	X	0	R7 = R8 sll 4
2	7	8	7	1	0	x	1	1	0	x	0	x	0	0	x	0	R7 = R7 – R8
3																	

Part B (12 points) Compute mem[3000] + 20 and store the result in mem[4000].

#	X	Y	Z	rwe	im en	im va	au en	-a /s	lu en	lf	su en	st	ld en	st en	r/ -w	msel	description
1	x	x	7	1	1	3000	0	x	1	C	0	x	0	0	x	0	R7 = 3000
2	7	x	7	1	0	x	0	x	0	x	0	x	1	0	1	1	R7 = Mem[3000]
3	7	x	7	1	1	14	1	0	0	x	0	x	0	0	x	0	R7 = R7 + 20
4	x	x	8	1	1	4000	0	x	1	C	0	x	0	0	x	0	R8 = 4000
5	8	7	x	0	0	x	0	x	0	x	0	x	0	1	0	1	Mem[4000] = R7
6																	

Part C (8 points) Register 7 holds two packed 16 bit binary strings A and B as illustrated below.

A		B	
31	16	15	0

Write a microcode sequence that unpacks A and B and computes $R_8 = A \oplus B$.

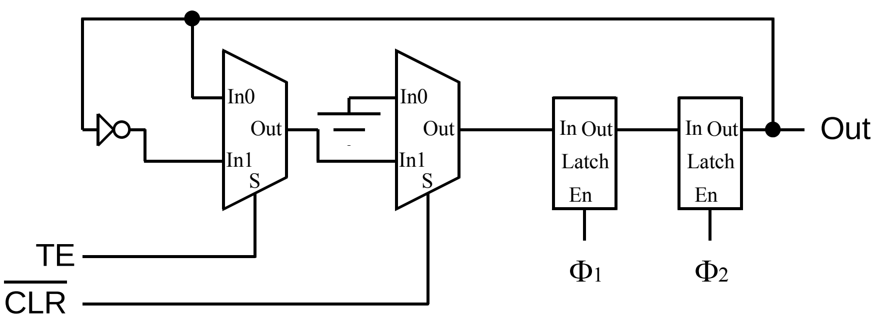
#	X	Y	Z	rwe	im en	im va	au en	-a /s	lu en	lf	su en	st	ld en	st en	r/ -w	msel	description
1	7	x	8	1	1	FFFF	0	X	1	8	0	x	0	0	x	0	R8 = R7 and FFFF
2	7	x	7	1	1	10	0	x	0	x	1	0	0	0	x	0	R7 = R7 srl 16
3	7	8	7	1	0	x	0	x	1	6	0	x	0	0	x	0	R8 = R7 xor R8
4																	

Assuming A and B are nonzero, what must be true about A and B for the result in R_8 to be zero?

A = B

Problem 4 (2 parts, 20 points) Counters

Part A (10 points) Design a toggle cell using two transparent latches, two 2 to 1 muxes, and one inverter. Your toggle cell should have an active high toggle enable input **TE**, and an active low clear input $\overline{CLR}$, clock inputs Φ_1 and Φ_2, and an output **Out**. The $\overline{CLR}$ signal has precedence over **TE**. Label all signals. Also complete the behavior table for the toggle cell.



TE	$\overline{CLR}$	CLK	Out
0	0	↑↓	0
1	0	↑↓	0
0	1	↑↓	Q_0
1	1	↑↓	$\overline{Q_0}$

Part B (10 points) Now combine these toggle cells to build a **divide by seven** counter. Your counter should have an external clear, external count enable, and three count outputs O_2, O_1, O_0. Use any basic gates (AND, OR, NAND, NOR, XOR & NOT) you require. Assume clock inputs to the toggle cells are already connected. Your design must support multi-digit systems.