Problem 1 (25 points)
Here is some information about the 2114 RAM chip, which was used for video color RAM in the Commodore 64.

a) How many words of memory does this chip contain?

$$
2^{10}=1 k=1024
$$

b) How many bits are in each word?
c) In the block diagram, the memory array is described as 64 rows and 64 columns. Is that referring to the words or to the bit cells?

d) How would the memory array be described if it was the opposite of your answer from \#3? I.e. if you said it was referring to the bit cells, what would the description be if it was referring to the words, and vice versa.
64 cows $\times 16$ columns
e) If a different chip contained four times as many words, how many additional address pins would be needed? Two more
f) Based on the block diagram, what combinations) of $\bar{S}$ and $\bar{W}$ will tri-state the I/O pins? Assume that the ristate drivers are active when their control signal is 1 .


Problem 2 (10 points)

a) Based on the memory devices we've seen in this class, what is an appropriate name for the signal marked with a question mark in the bottom left of the diagram?
Chip select, chip enable, output enable, etc.
b) Color in the cells in the diagram above that contain the data at address 6 .

The datapath reference is on the last page. You can tear it off if you want.
Problem 3 ( 15 points)
In the MIPS datapath, all of the following effectively implement R2 = R1:

- R2 = RI OR 0
- R2 = R1 OR RD
- R2 = R1 + 0
- R2 = R1 + RD
- Setting st_en and Id_en to 1, disabling the arithmetic, logic, and shift units and memory, and using the $Y$ bus to transfer R1 to R2.

Describe two other unique ways to accomplish R2 = R1 in the MIPS datapath. You can use existing instructions, or you can describe what the datapath components should do or what the control signals should be.

$$
\begin{aligned}
& \text { shift by } 0 \\
& \text { AND with FFFFFFFF } \\
& \text { Xor with } 0 \\
& \text { set LF to identity }
\end{aligned}
$$

The datapath diagram is on the last page. You can tear it off if you want.

## Problem 4 ( 25 points)

4a) Use the description column to fill in the datapath signals to implement that operation.

| X | Y | Z | rwe | $\begin{aligned} & \text { im } \\ & \text { en } \end{aligned}$ | im_va | $\begin{aligned} & \text { au } \\ & \text { en } \end{aligned}$ | $\begin{aligned} & -\mathrm{a} \\ & \mathrm{I} \end{aligned}$ | $\begin{aligned} & \text { lu } \\ & \text { en } \end{aligned}$ | $\mathrm{If}_{3-0}$ | su | st | st en | $\begin{aligned} & \text { Id } \\ & \text { en } \end{aligned}$ | $\begin{aligned} & -r \\ & \text { /w } \end{aligned}$ | msel | description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 3 | 7 |  | 0 | 0 |  | 0 |  | 0 |  | $\bigcirc$ |  | 1 | $\bigcirc$ | 1 | 1 | MEM[R3] = R7 |
| 2 |  | 7 | 1 | 1 | $-3$ | 0 |  | 0 |  | 1 | 0 | 0 | O | 0 | $\bigcirc$ | R7 $=$ R2 SRL 3 |

4b) From the provided microcode, write a description of the operation, either as an assembly code instruction or as a plain-English description. Simplify the description of the operation if possible - for example, like in problem 3, if the datapath performs R2 = R1 OR 0 , it would be better to write R2 = R1 or "R2 gets the value of R1". Note that everything not bolded is the same in all rows. Remember that the immediate is sign-extended.

| X | Y | Z | rwe | im en | im_va | $\begin{aligned} & \text { au } \\ & \text { en } \end{aligned}$ | $\begin{aligned} & \text {-a } \\ & \text { /s } \end{aligned}$ | lu en | Lf ${ }_{3-0}$ | $\begin{aligned} & \text { su } \\ & \text { en } \end{aligned}$ | st | $\begin{aligned} & \text { st } \\ & \text { en } \end{aligned}$ | Id en | $\begin{aligned} & \text {-r } \\ & \text { /w } \end{aligned}$ | msel | description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 3 | 2 | 1 | 1 | 1 | FFFF $_{16}$ | 0 | 0 | 1 | 1110 | 0 | 0 | 0 | 0 | 0 | 0 | set Rl to all Is |
| 3 | 2 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1111 | 0 | 0 | 0 | 0 | 0 | 0 | set RI to all $I_{s}$ |
| 3 | 2 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | $R 1=R 3$ |
| 3 | 2 | 1 | 1 | 0 | FFFF $_{16}$ | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | $R 1=R 3+R 2$ |

## Problem 5 (25 points)

- Assume that R1 contains a value between 0 and 31, and consider that the "input" to the code.
- The "output" is in R5 after the code completes.

$$
\begin{array}{ll}
\text { R2 }=32 & \# \\
\text { R2 }=\text { R2 - R1 } & \# \\
\text { R5 }=-1 & \# \\
\text { RS }=\text { RS SRI R2 } & \# \text { shift by amount stored in R2 }
\end{array}
$$

a) Describe the result of the code in terms of the input and output. Hint: the operation is mathematical in nature, although it can be also described in terms of the bits if you don't see the mathematical connection.

$$
\begin{aligned}
& \text { Puts } 2^{R 1}-1 \text { in } R 5 \\
& \text { Eng. if } R 1=4, R 3=0 \ldots 01111
\end{aligned}
$$

b) The author of the code forgot that the shift amount for the MIPS shifter is 5 bits (refer to the datapath reference). It comes from the least-significant 5 bits of the $Y$ bus. How does that affect the behavior of the code for the intended input range of 0-31?
(note that you can ignore any related incorrect behavior in your answer to part a)


## Bonus (1 possible bonus point)

If you've finished early, fix the code so that it works for all input values 0-31. You can write actual code, or you can describe the fix as long as it's clear how it would be translated to assembly code.
split the shift into multiple shifts when reedel.


| Signal | Description | Signal | Description |
| :--- | :--- | :--- | :--- |
| $X, Y$ | Read register addresses | If | Logic function (see table below diagram)) |
| $Z$ | Write register address | su_en | Shift unit enable |
| rwe | Register write enable | st | Shift type (see table below diagram) |
| im_en | Immediate enable | st_en | Store enable |
| im_va | Immediate value | Id_en | Load enable |
| au_en | Arithmetic unit enable | -r/w | Read/write memory (0=read, $1=$ write) |
| -a/s | Add/subtract ( $0=a d d, 1=$ subtract) | msel | Memory select (memory output enable) |
| lu_en | Logic unit enable |  |  |


| instruction | RTL description |
| :---: | :---: |
| add | \$d = \$ $\mathrm{s}+\mathrm{\$ t}$; |
| subtract | \$d = \$s - \$t; |
| add immediate | \$t = \$ s + imm; |
| and | \$d = \$s AND \$t; |
| or | \$d = \$s OR \$t; |
| xor | \$d = \$s XOR \$t; |
| and immediate | \$t = \$s AND imm; |
| or immediate | \$t = \$s OR imm; |
| xor immediate | \$t = \$s XOR imm; |
| shift left logical | \$d = \$ t SLL a; |
| shift right logical | \$d = \$t SRL a; |
| shift left arithmetic | \$d = \$t SLA a; |
| shift right arithmetic | \$d = \$t SRA a; |
| load word | \$t = MEM[\$s]; |
| store word | MEM[\$s] = \$t; |
| load immediate | \$t = imm; |
| branch if equal | IF \$s = \$t GOTO label; |
| branch if not equal | If \$s != \$t GOTO label; |
| set if less than | \$d = \$s < \$t; (if \$ < \$t \$d = 1; else \$d = 0;) |
| set if less than immediate | \$d = \$s < imm; (if \$s < imm \$t = 1; else \$t = 0;) |
| jump | GOTO label; |

