ECE2020 A Fall 2018 Test 3

Name: _____

- Only a writing implement may be used on this exam (i.e. no books, notes, or any electronics).
- If the meaning of any question is not clear, please ask for clarification.
- Partial credit can only be awarded for work shown.

Honor pledge:

On my honor, I pledge that I will neither receive nor provide improper assistance in the completion of this test. I understand and accept my responsibility as a member of the Georgia Tech Community to uphold the Honor Code at all times, and I know that I have options for reporting honor violations at osi.gatech.edu.

GTID: _____ Signature: _____

Boolean Identities

Identity	$A + 0 = A$	$A \cdot 1 = A$
Dominance	$A + 1 = 1$	$A \cdot 0 = 0$
Idempotence	$A + A = A$	$A \cdot A = A$
Inverse	$A + \overline{A} = 1$	$A \cdot \overline{A} = 0$
Commutative	$A + B = B + A$	$A \cdot B = B \cdot A$
Associative	$A + (B + C) = (A + B) + C$	$A \cdot (B \cdot C) = (A \cdot B) \cdot C$
Distributive	$A \cdot (B + C) = A \cdot B + A \cdot C$	$A + B \cdot C = (A + B) \cdot (A + C)$
Absorption	$A \cdot (A + B) = A$	$A + A \cdot B = A$
DeMorgan's	$\overline{(A + B)} = \overline{A} \cdot \overline{B}$	$\overline{(A \cdot B)} = \overline{A} + \overline{B}$
Double Complement	$\overline{\overline{A}} = A$	
FOIL	$(A + B) \cdot (C + D) = A \cdot C + A \cdot D + B \cdot C + B \cdot D$	
Disappearing opposite	$A + \overline{A} \cdot B = A + B$	

Decimal	Binary	Hex
0	0	0
1	1	1
2	10	2
3	11	3
4	100	4
5	101	5
6	110	6
7	111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

2^{-6}	0.015625
2^{-5}	0.03125
2^{-4}	0.0625
2^{-3}	0.125
2^{-2}	0.25
2^{-1}	0.5
2^{0}	1
2^{1}	2
2^{2}	4
2^{3}	8
2^{4}	16
2^{5}	32
2^{6}	64
2^{7}	128
2^{8}	256
2^{9}	512
2^{10}	1024

8-channel Multiplexer (inputs A_{7-0}, output Q

S2	S1	S0	Q
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

3-to-8 Line Decoder with Enable

A2	A1	A0	EN	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0
X	X	X	0	0	0	0	0	0	0	0	0

8-channel Demultiplexer (input A, outputs Q_{7-0})

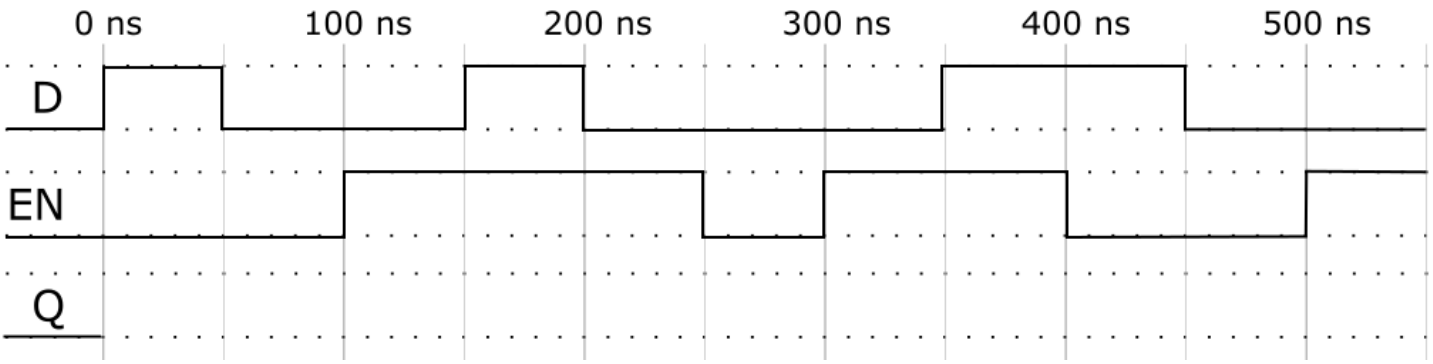
S2	S1	S0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	A
0	0	1	0	0	0	0	0	0	A	0
0	1	0	0	0	0	0	0	A	0	0
0	1	1	0	0	0	0	A	0	0	0
1	0	0	0	0	0	A	0	0	0	0
1	0	1	0	0	A	0	0	0	0	0
1	1	0	0	A	0	0	0	0	0	0
1	1	1	A	0	0	0	0	0	0	0

8-to-3 Priority Encoder (Priority A7->A0) with valid indicator

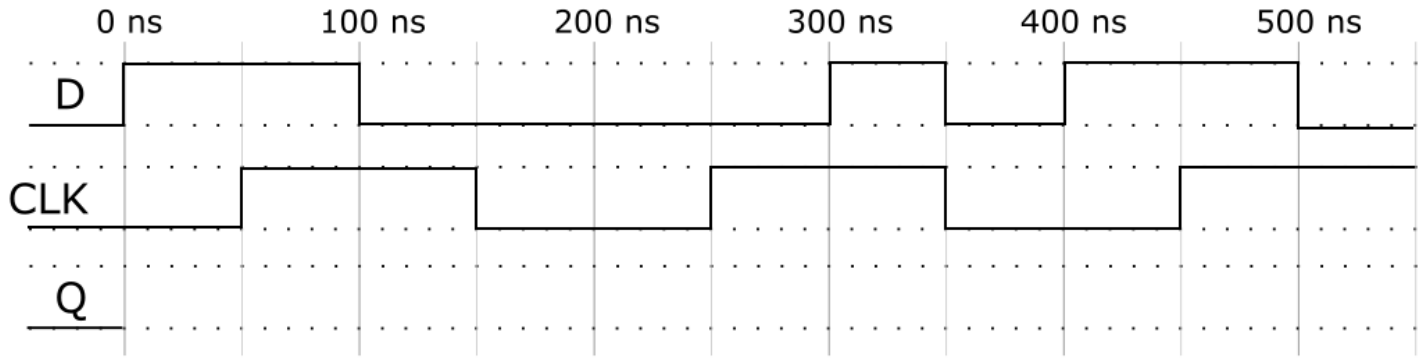
A7	A6	A5	A4	A3	A2	A1	A0	E2	E1	E0	V
1	X	X	X	X	X	X	X	1	1	1	1
0	1	X	X	X	X	X	X	1	1	0	1
0	0	1	X	X	X	X	X	1	0	1	1
0	0	0	1	X	X	X	X	1	0	0	1
0	0	0	0	1	X	X	X	0	1	1	1
0	0	0	0	0	1	X	X	0	1	0	1
0	0	0	0	0	0	1	X	0	0	1	1
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0

Problem 1 (20 points)

Simulate the output behavior of a D latch that is driven with the following input. The output is low at the beginning, as shown. Assume that the latch propagation delay (D to Q and EN to Q) is 20 ns. Note that each dot on the waveform is 10 ns.



Simulate the output behavior of a D flip-flop that is driven with the following input. The output is low at the beginning, as shown. Assume that the flip-flop propagation delay (clk to Q) is 20 ns and the setup and hold times are each 10 ns. Note that each dot on the waveform is 10 ns.



Problem 2 (30 points)

Create a **state diagram** for a state machine that implements the following description.

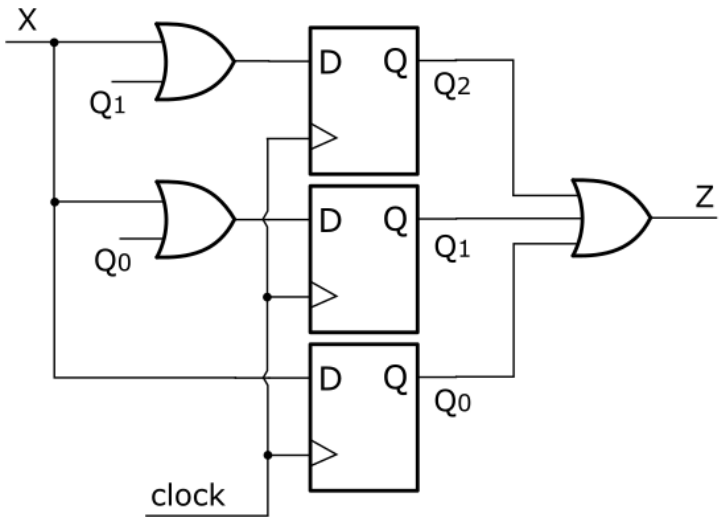
The state machine has two inputs, HOT and COLD, which indicate that an oven is too hot or too cold. Both inputs will never be asserted together, and if neither is asserted, then the temperature is correct.
The state machine has two Moore outputs, BURN and VENT. If BURN is asserted, a flame lights to heat up the oven, and if VENT is asserted, a vent opens to cool the oven. Both outputs should never be asserted at the same time.

If COLD is high, the flame should light as soon as possible, and if HOT is high, the vent should open as soon as possible. However, once lit, the flame must remain lit for at least two seconds. Other than that, it should not be lit any longer than necessary (nor should the vent be open any longer than necessary, and the vent has no requirement to stay open).

Assume that the state machine is clocked once per second, so you can use state transitions to keep track of time (and thus do not need any "time" input).

Problem 3 (30 points)

The following state machine has one input (X), three state bits ($Q_{2\text{-}0}$), and one output (Z).



The designer had four states, and chose the following state encodings:

State Name	Encoding ($Q_{2\text{-}0}$)
Eeny	000
Meeny	111
Miney	110
Moe	100

1) During which state(s) is the output Z asserted?

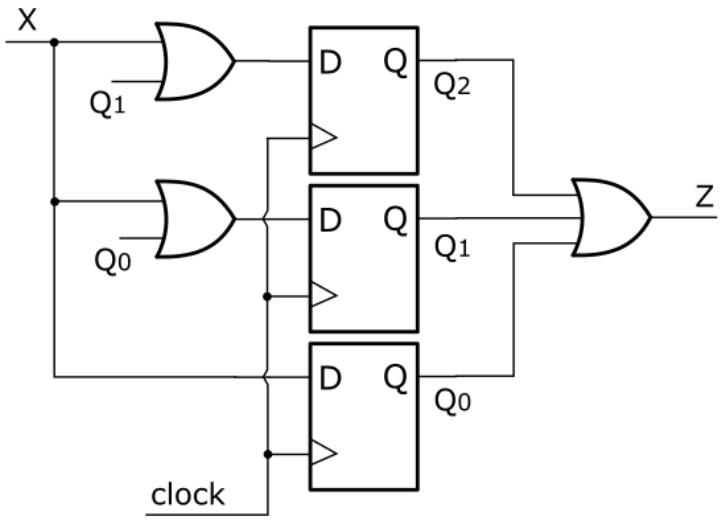
2) If the current state is Meeny and the input is 1, what will the next state be?

3) Complete the blank entries in the following portion of the state machine's transition table.

Current State	**$Q_{2\text{-}0}$**	**Input**	**Next State**	**$Q_{2\text{-}0}^{+}$**	**Z**
Eeny	000	0			
Eeny	000	1			
Moe	100	1			

Problem 4 (20 points)

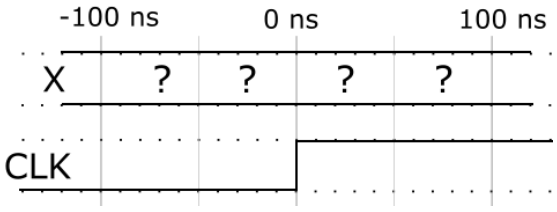
The state machine from the previous problem is repeated here, along with some timing parameters of the devices involved.



Flip-flop propagation delay	70 ns
Flip-flop setup time	15 ns
Flip-flop hold time	10 ns
2-input OR propagation delay	30 ns
3-input OR propagation delay	45 ns

1) Based on the provided parameters, what is the minimum amount of time allowed between successive rising clock edges? Express your answer as a sum of numbers; you don't need to actually sum them into a final value.

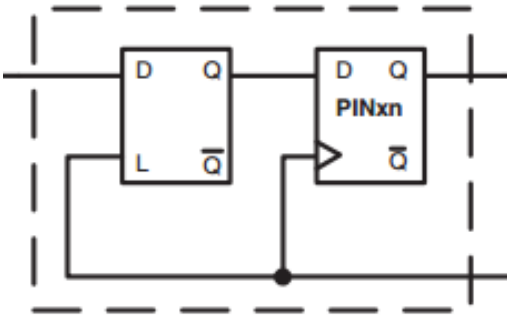
2) [The image below is to help visualize this question] If a rising edge of the clock occurs at t=0, during what period(s) of time must the X input <u>not</u> change to avoid violating any timing requirements? Express your answer as one or more intervals around 0; for example -5 ns to 15 ns.



Bonus Question (up to 1 point)

All of this is only worth up to 1 point. **Do not bother with this unless you are finished with everything else.**

Observe the following circuit. It has an input, an output, and a clock signal, and consists of a latch and a flip-flop.



The input (signal on the left) can change at any time with respect to clock edges.

What relationship(s) between parameters of the latch and flip-flop must be true to ensure that all timing requirements are met?