ECE 2020

Digital Systems Design

Quiz IV

November 29, 2012

This quiz is closed book and closed note and no calculators.

There are four questions. Do read them over before you start to work. If you need to make any assumptions, state them.

The meaning of each question should be clear, but if something does not make any sense to you, please ask for clarification. If you run out of room, please continue on the back of the previous page.

Good Luck!

Name (Please print)_____

This quiz will be conducted according to the Georgia Tech Honor Code. I pledge to neither give nor receive unauthorized assistance on this exam and to abide by all provisions of the Honor Code.

Signed_____

Question	Score	Max
1		20
2		30
3		30
4		20
Total		**100**

1. (20) Logic and barrel shifter units

    (a) (5) What is the result of an arithmetic right shift by 10 bits of (the half word) 0xA752.

    (b) (5) What is the result of a rotate left by 8 bits of (the half word) 0x3D7F.

    (c) (10) Show the design for one bit of a logic unit which can compute any function of two boolean variables (as designed in class). You may build the unit out of any multiplexor, decoder, or encoder module, or any gates you need. Show how to configure your design to compute the function $z = x + \overline{y}$. You must show what signals or values are connected to which pin of your design. You must label each pin inside the module.

2. (30) Memory

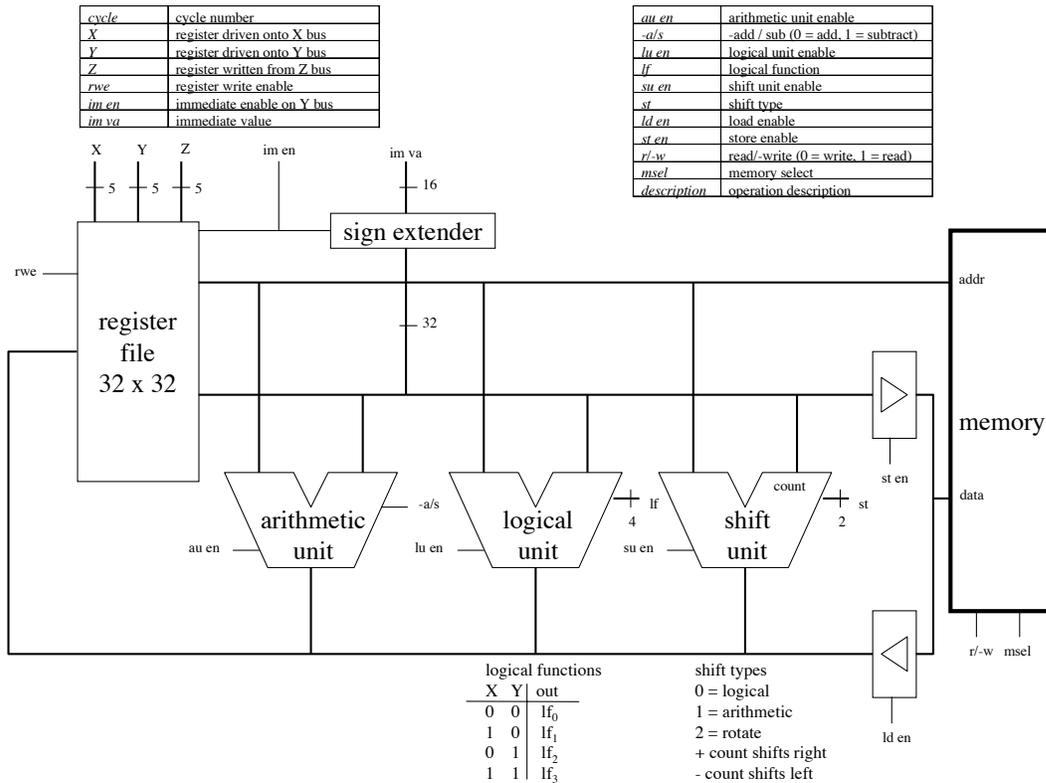(a) (5) Consider a 4Kx4 memory chip. Suppose there are 128 bits per row? What is the specification of the column mux?

(b) (5) For the chip in (a), what is the specification of the row decoder?

(c) (5) Which is more dense (bits/area), SRAM or DRAM? Why?

(d) (15) Design a 128Kx16 memory out of 32Kx4 chips. You must identify all address, data, and control bits/busses and their connections for full credit.

3. (30) ISA/Datapath

cycle	cycle number
X	register driven onto X bus
Y	register driven onto Y bus
Z	register written from Z bus
rwe	register write enable
im en	immediate enable on Y bus
im va	immediate value

au en	arithmetic unit enable
-a/s	-add / sub (0 = add, 1 = subtract)
lu en	logical unit enable
lf	logical function
su en	shift unit enable
st	shift type
ld en	load enable
st en	store enable
r/-w	read/-write (0 = write, 1 = read)
msel	memory select
description	operation description

logical functions

X	Y	out
0	0	lf_0
1	0	lf_1
0	1	lf_2
1	1	lf_3

shift types
0 = logical
1 = arithmetic
2 = rotate
+ count shifts right
- count shifts left

Xra	Yra	Zwa	rwe	im en	im va	au en	a/s	lu en	LF	su en	ST	st en	ld en	r/~w	msel

a) (20) Write the microcode for the following sequence of RTL statements in the table above. **Register addresses and immediate values should be in hex. All other fields must in binary and be the correct number of bits.** Assume that register i (Ri) is initialized to i. Assume that all arithmetic operands are signed (twos complement) numbers.

R7 = R11 + R13
R2 = R5 AND R7
MEM[R8] = R2
R11 = R12/4 (division by 4)

b) (5) What is the value of the data that is loaded into Mem[8]? _____

c) (5) What is the final value in R11? _____

4. (20) Instruction Set Architecture

a) Consider the MIPS assembly language statement: addi $12, $4, –7

   If the opcode for addi is 010110, what is the hexadecimal encoding of this instruction? Show the encoding of each field and the overall hex encoding.

b) Consider the MIPS assembly language statement: XOR $16, $24, $8

   If the opcode for XOR is 100100, what is the hexadecimal encoding of this instruction? Show the encoding of each field and the overall hex encoding.

c) In a couple of sentences, why is R0 = 0 in MIPS (why did the architects decide to do this)?

d) What is the rationale for immediate type instructions.