# ECE 2020

## Digital System Design

# Quiz II

October 9, 2012

This exam is closed book and closed note and no calculators.

There are five questions and an extra credit. Do read them over before you start to work. If you need to make any assumptions, state them.

The meaning of each question should be clear, but if something does not make any sense to you, please ask for clarification. If you run out of room, please continue on the back of the previous page.

## Good Luck!

Name (Please print)_____

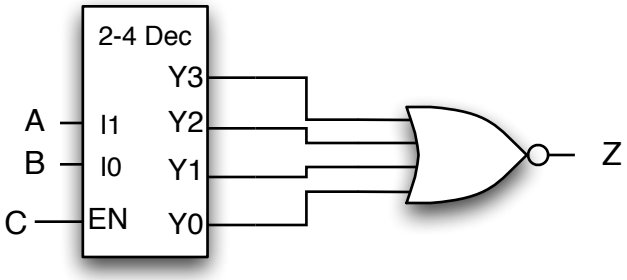
This exam will be conducted according to the Georgia Tech Honor Code. I pledge to neither give nor receive unauthorized assistance on this exam and to abide by all provisions of the Honor Code.

Signed_____

| Question | Score | Max |
|---|---|---|
| 1 | | 20 |
| 2 | | 20 |
| 3 | | 20 |
| 4 | | 20 |
| 5 | | 20 |
| 6 (EC) | | 10 |
| **Total** | | **110** |

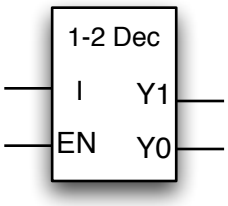
1. (20) Decoders

a) (10) For the circuit shown, write a minimum expression for Z as a function F(A,B,C). (Hint: Think!)

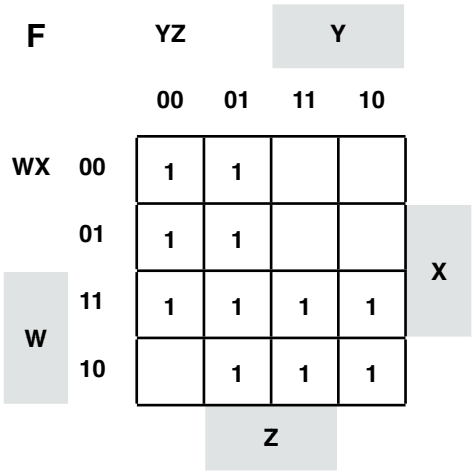



Z =

b) (10) Design a 2-4 decoder **with enable** using 1-2 decoders (as many as you need), and a minimum number of additional gates if necessary. Use the decoder symbol as given, and duplicate as many times as needed. All signals (inputs $I_{1:0}$ , EN, and outputs $Y_{3:0}$) must be labeled correctly.

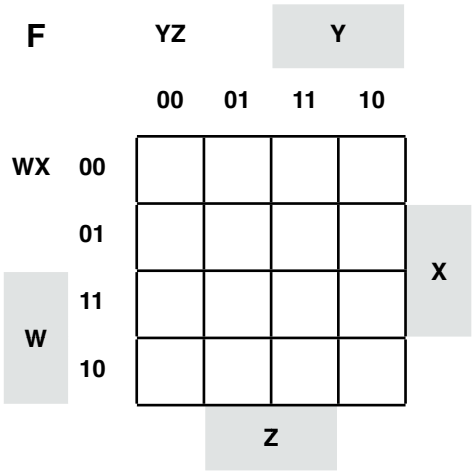


2. (20) Logic minimization




a) List **all** prime implicants for the function in the k-map above.

b) Complete the k-map below and find a mimimum **product of sums** expression for the function $F = X\overline{Y} + WX + \overline{X}Y\overline{Z} + \overline{W}XY$.



2. (20) Multiplexors and more.

   a) (10) Design a **2-2X1** multiplexor using **only** T-gates and minimum number of inverters. Label all signals.

   b) (10) Design an 4x1 mux using 2x1 muxes and a minimum amount of additional logic as needed. Label the 4x1 muxes with inputs $I_3$, $I_2$, $I_1$ and $I_0$, output Y, and the correct control inputs $S_i$.

3. (20) Consider a 4-2 priority encoder, with the priority order is {3,2,1,0}. For each input $I = I_3 I_2 I_1 I_0$, **given in hex**, what are the outputs?

a) I =A

| Y1 | Y0 | V |
|---|---|---|
| | | |

b) I=0

| Y1 | Y0 | V |
|---|---|---|
| | | |

c) I=4

| Y1 | Y0 | V |
|---|---|---|
| | | |

d) I=F

| Y1 | Y0 | V |
|---|---|---|
| | | |

e) I=6

| Y1 | Y0 | V |
|---|---|---|
| | | |

4. (20) (20) Adder/Subtractor. You are given A and B and that V(A) and V(B) are respectively the actual decimal values that A and B encode. Suppose that A, B, and $\overline{a}/s$ (read $\overline{add}/sub$) are inputs to an 5-bit adder/subtractor as designed in class. For each row of this table give (1) the 5-bit binary output of the adder/subtractor S, (2) the values of V(S) = V(A) op V(B), and whether or not overflow occurs. Op is either + or − as indicated. If overflow does occur, write (the values of) V(S) ≠ V(A) op V(B). Note that V(x) depends on whether the numbers are unsigned or signed.

a) Assume A and B are unsigned numbers:

| A | B | $\overline{a}/s$ | S | V(S) = V(A) op V(B) | Overflow? |
|---|---|---|---|---|---|
| 10101 | 11010 | 0 | | | |
| 10101 | 11010 | 1 | | | |

b) Assume A and B are signed twos complement numbers:

| A | B | $\overline{a}/s$ | S | V(S) = V(A) op V(B) | Overflow? |
|---|---|---|---|---|---|
| 10101 | 11010 | 0 | | | |
| 10101 | 11010 | 1 | | | |

5. (+10) Extra Credit. Design a 16-4 priority encoder using 4-2 encoders and additional modules/ gates. Lower indices should have higher priority.