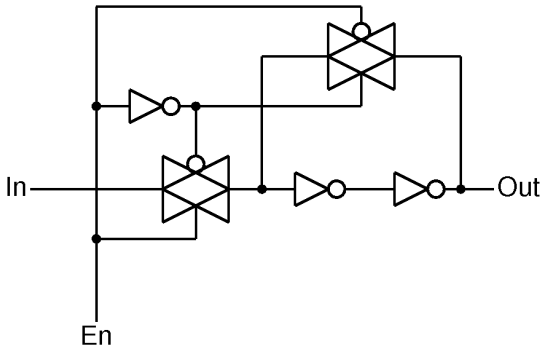
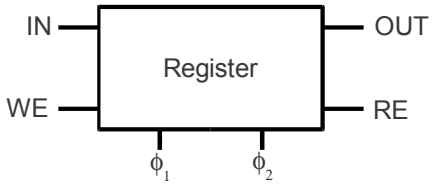
Problem 1 (3 parts, 21 points) State

Part A (8 points) Implement a transparent latch using only inverters and pass gates. Label the inputs **In** and **En**, and output **Out**.

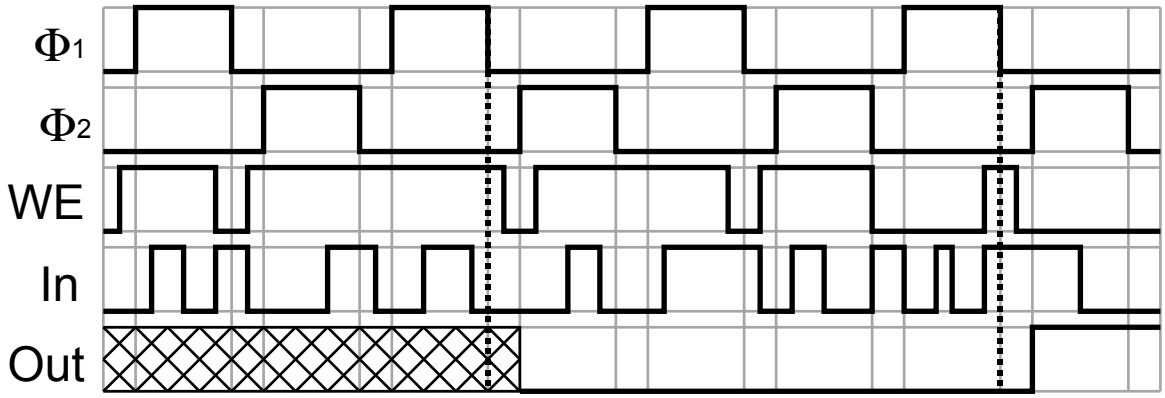


Part B (7 points) Consider a register with a selectable *write enable* (WE) and *read enable* (RE). It is implemented with transparent latches, a 2 to 1 mux, and a pass gate. Describe its behavior by completing the output values. Also indicate when a write and/or a read is being performed.



IN	WE	RE	CLK	OUT	write?	read?
A	0	0	↑↓	Zo		
A	1	0	↑↓	Zo	✓	
A	0	1	↑↓	Qo		✓
A	1	1	↑↓	A	✓	✓

Part C (6 points) Assume the following signals are applied to a register with write enable Draw the output signal **Out**. Draw a vertical line where **In** is sampled. *Draw crosshatch where **Out** is unknown.*



Problem 2 (4 parts, 40 points) Number Representations & Arithmetic

Part A (10 points) Convert the following notations:

decimal notation		binary notation
327	⇨	**101000111**
37.5625	⇦	100101.1001
44.125	⇨	**101100.001**
octal notation		**hexadecimal notation**
73.37	⇨	**111011.0110111 = 3B.7C**
1011010.1101 = 132.64	⇦	0x5A.D

Part B (12 points) For these 12 bit representations, determine the most positive value and the step size (difference between sequential values).**All answers should be expressed in decimal notation**.Fractions (e.g., 3/16ths) may be used. All signed representations are two's complement.

representation	most positive value	step size
unsigned integer (12 bits) . (0 bits)	**4K**	**1**
signed fixed-point (6 bits) . (6 bits)	**31 63/64**	**1/64**
unsigned fixed-point (8 bits) . (4 bits)	**255 15/16**	**1/16**
signed fixed-point (10 bits) . (2 bits)	**511 3/4**	**1/4**

Part C (6 points) A 29 bit floating point representation has a 17 bit mantissa field, a 11 bit exponent field, and one sign bit.

What is the largest value that can be represented (closest to infinity)? 2^{1023}

What is the smallest value that can be represented (closest to zero)? 2^{-1024}

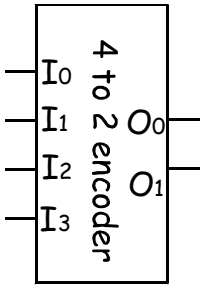
How many decimal significant figures are supported? **5**

Part D (12 points) For each problem below, compute the operations using the rules of arithmetic, and indicate whether an overflow occurs assuming all numbers are expressed using a **six bit unsigned fixed-point** and **six bit two's complement fixed-point** representations.

	1010.00 + 111.11		110.11 + 10.00		1001.01 - 1100.10		101.11 - 100.01	
result	**1.11**		**1000.11**		**1100.11**		**1.10**	
unsigned error?	□ no	■ yes	■ no	□ yes	□ no	■ yes	■ no	□ yes
signed error?	■ no	□ yes	□ no	■ yes	■ no	□ yes	■ no	□ yes

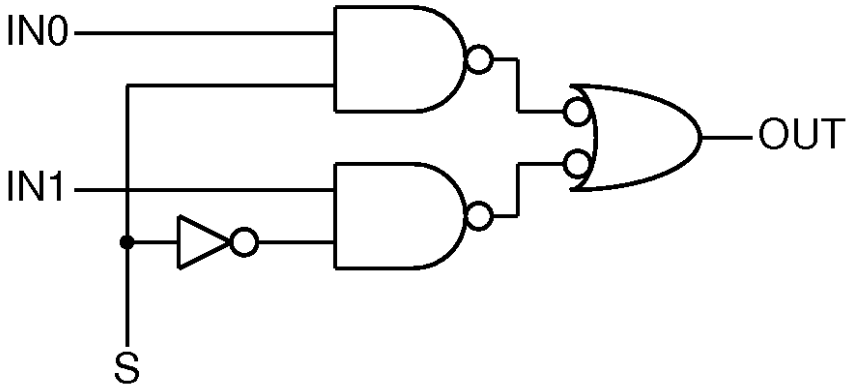
Problem 3 (2 parts, 15 points) Building Blocks

Part A (7 points) Complete the following truth table for a priority encoder. Assume the priority order (from highest to lowest) is $I_2 > I_0 > I_3 > I_1$



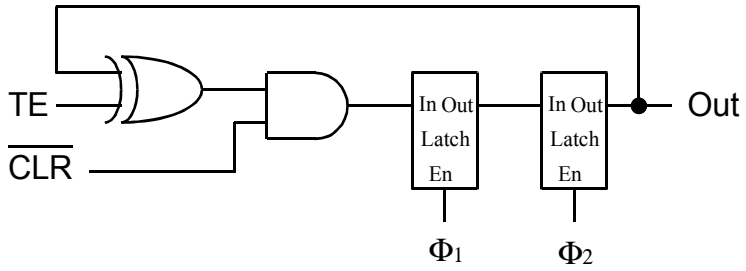
I_0	I_1	I_2	I_3	V	O_1	O_0
0	**0**	**0**	**0**	0	X	X
1	**X**	**0**	**X**	1	0	0
0	**1**	**0**	**0**	1	0	1
X	**X**	**1**	**X**	1	1	0
0	**X**	**0**	**1**	1	1	1

Part B (8 points) Implement a 2 to 1 multiplexer using only basic gates (AND, OR, NAND, NOR, NOT). Label all inputs and outputs.

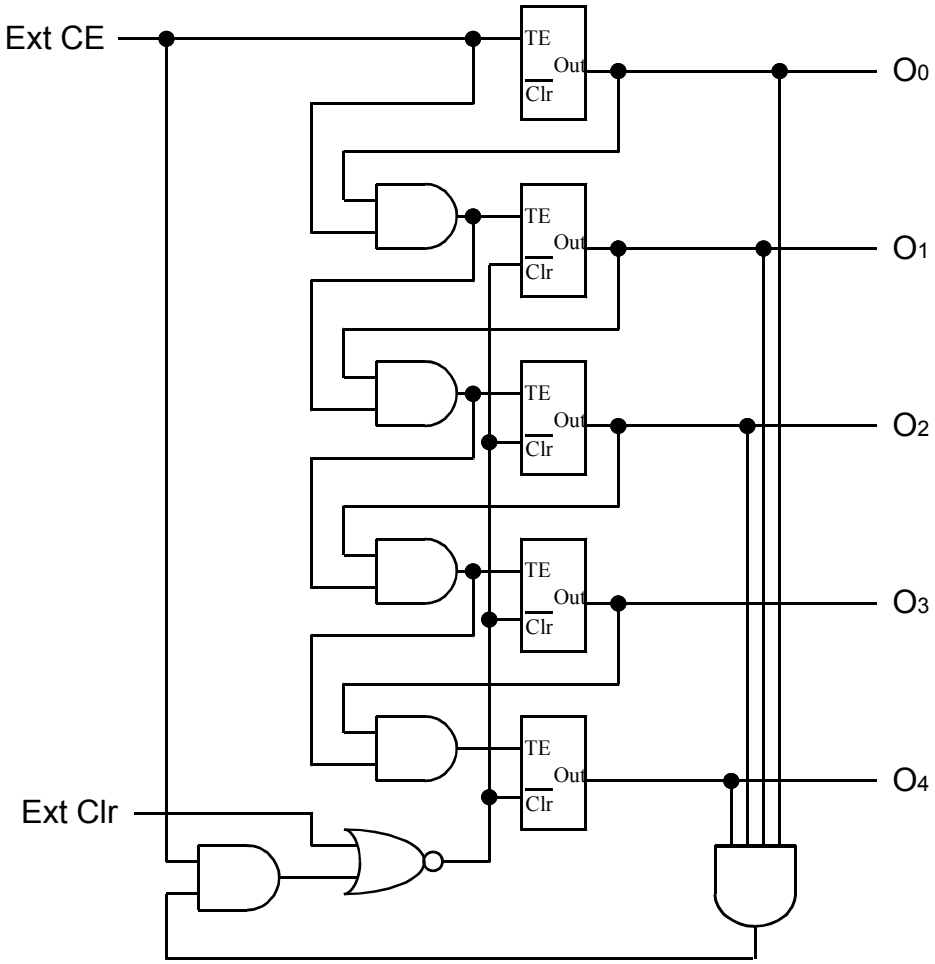


Problem 4 (3 parts, 24 points) Counters

Part A (7 points) Implement a toggle cell using ***only transparent latches and basic gates (XOR, AND, OR, NAND, NOR, NOT)***. Use an icon for the transparent latches. Label the inputs **TE**, $\overline{CLR}$ **,** $\mathbf{\Phi_1}$, $\mathbf{\Phi_2}$ and the output **Out**.



Part B (8 points) Now combine these toggle cells to build a **divide by 24** counter. Your counter should have an external clear, external count enable, and five count outputs O_4, O_3, O_2, O_1, O_0. Use any basic gates (AND, OR, NAND, NOR, & NOT) you require. Assume clock inputs to the toggle cells are already connected. *Your design should support multi-digit systems*.



Part C (9 points) Build a military timer (HH:MM) which displays hours (0...23) on the left and minutes (0...59) on the right as follows. In the diagram below:

a) Fill in the label "Divide by ___" on each counter.

b) Label the number of output wires coming from each counter to its attached display.

c) Draw the appropriate wiring connections to allow this military timer to correctly respond to external clear (Ext CLR) and count enable (Ext CE) signals, and to correctly increment the hour count when the maximum number of minutes have passed while the clock is still running.

Use any basic gates you require. Assume clock inputs are already connected.