Instructions: This is a closed book, closed note exam. Calculators are not permitted. If you have a question, raise your hand and I will come to you. Please work the exam in pencil and do not separate the pages of the exam. For maximum credit, show your work.
Good Luck!

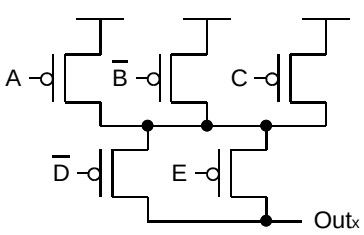
Your Name (***please print***) _____

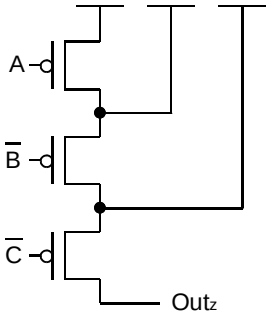
1	2	3	4	total
30	18	28	24	100

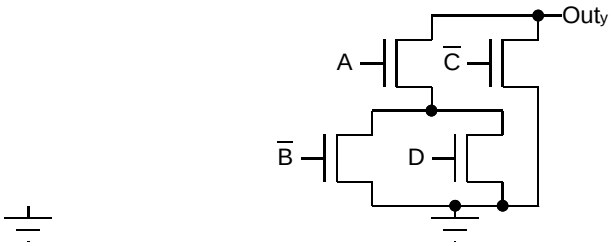
Binary Racer

Problem 1 (3 parts, 30 points) Incomplete Circuits

For each partial switch circuit below, complete the complementary switching network so the circuit contains no floats or short. Also write the Boolean expression computed by the completed circuit. Assume the inputs and their complements are available.







OUTx =

OUTy =

OUTz =

Problem 2 (1 part, 18 points) Switch-Ready Expressions

Transform each of the following Boolean expressions to a form where they are ready for switch level implementation (i.e., there should only be bars over input variables, not over operations). The behavior of the expression should remain unchanged. **Do not implement**.

$Out_X = \overline{A \cdot \overline{B} + C} + \overline{D}$

$Out_Y = \overline{\overline{A} + \overline{\overline{B}} + \overline{C} \cdot D}$

$Out_Z = \overline{\overline{\overline{A} \cdot B} + \overline{C}}$

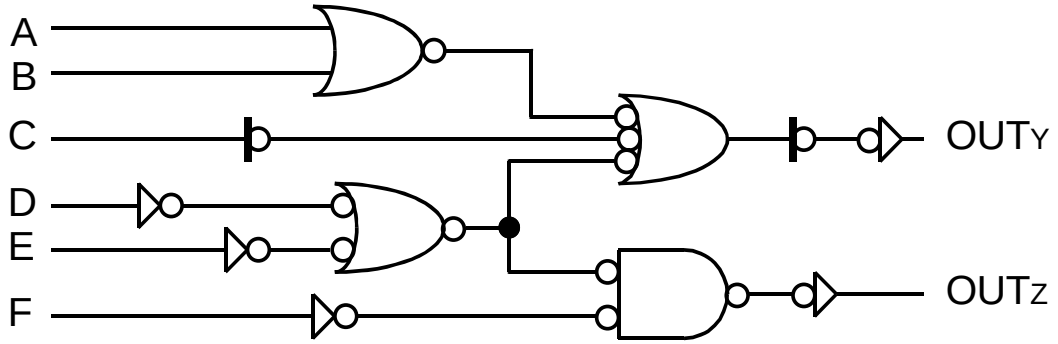
Problem 3 (3 parts, 28 points) Mixed Logic Design

Part A (10 points) Implement the following expression using multi-input **NAND** gates and inverters to minimize total transistors (switches) required. Use proper mixed logic design technique. Do not simplify the expression.

$$OUT_X = \overline{\overline{A} + B} + \overline{C} + (D + \overline{E}) \cdot F$$

switches =

Part B (8 points) Write the Boolean expression intended by the designer in for the mixed logic circuit below. Also determine the number of switches required for this implementation.



OUT_Y = _____

OUT_Z = _____

transistors = _____

Part B (10 points) Now reimplement this behavior using more efficient multi-input **NOR** gates and inverters. Your design must properly employ mixed logic methodology. Determine the number of switches required for this *improved* implementation.

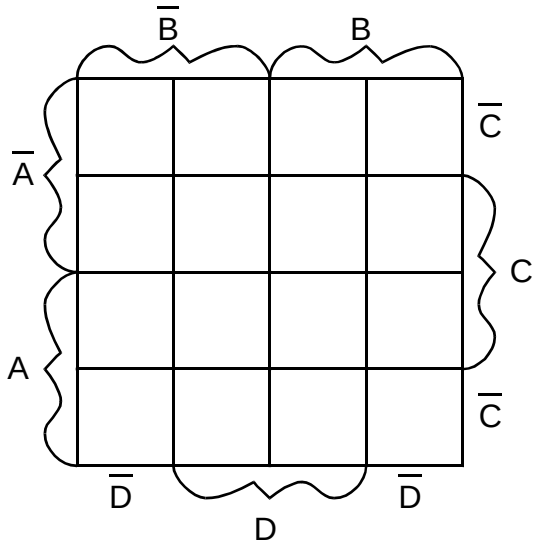
_____

transistors = _____

Problem 4 (2 parts, 24 points) Karnaugh Maps

Part A (12 points) For the follow expression, derive a simplified ***sum of products*** expression using a Karnaugh Map. Circle and list the prime implicants, indicating which are essential.

$$Out = (A + D) \cdot (A + \overline{B} + \overline{C}) \cdot (\overline{A} + \overline{B} + \overline{C} + \overline{D})$$

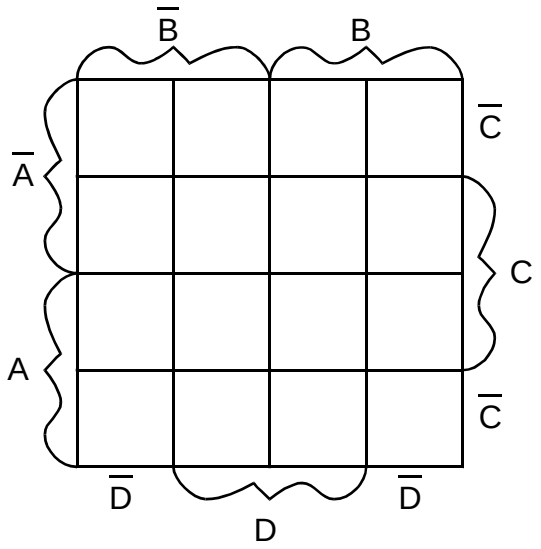


prime implicants	essential? yes	no
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐

simplified **SOP** expression _____

Part B (12 points) For the follow expression, derive a simplified ***product of sums*** expression using a Karnaugh Map. Circle and list the prime implicants, indicating which are essential.

$$Out = \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot C + B \cdot C \cdot \overline{D}$$



prime implicants	essential? yes	no
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐
	☐	☐

simplified **POS** expression _____