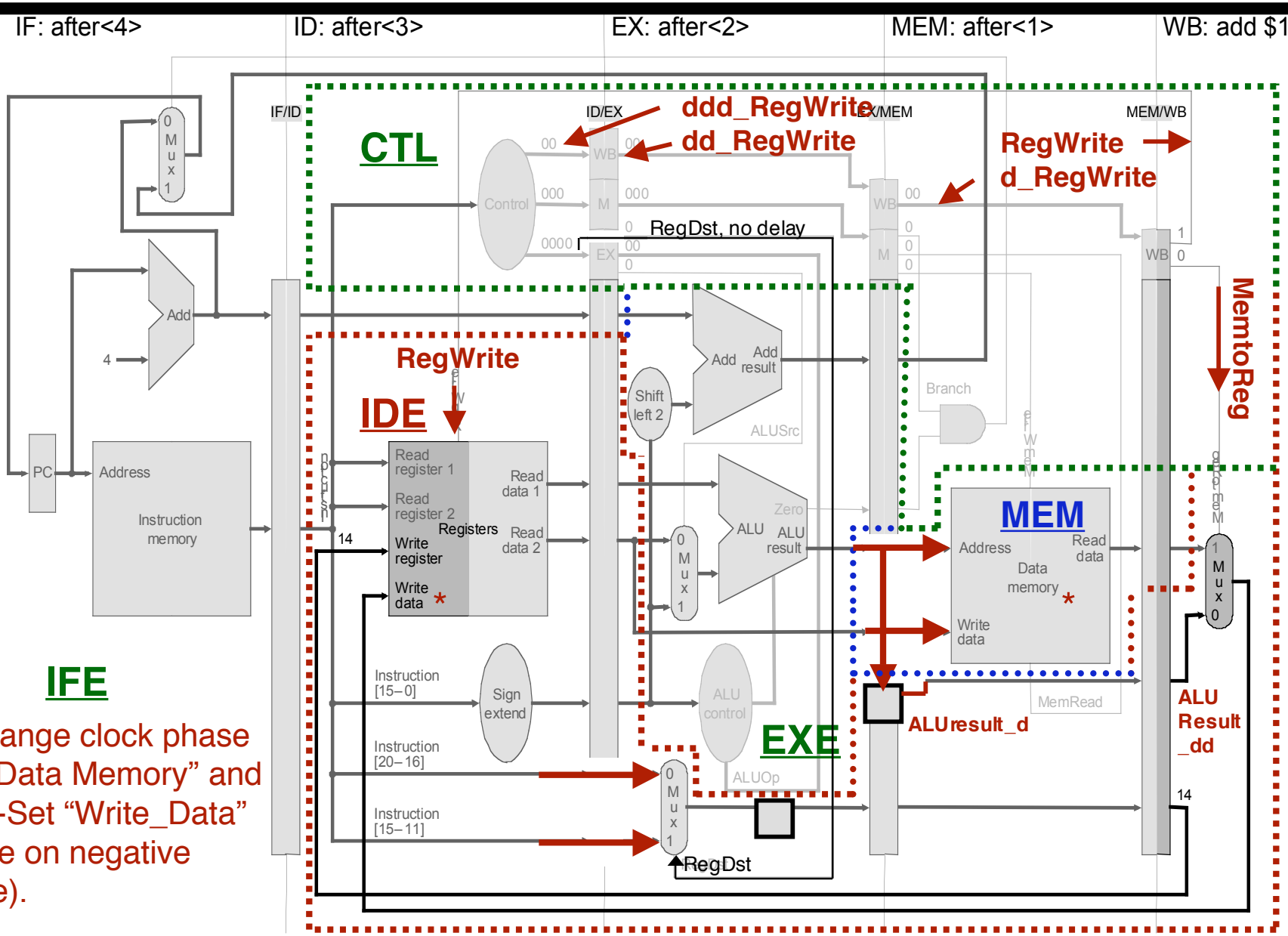
MIPS modules for Lab-3 and labeling delayed signals



* Change clock phase for “Data Memory” and Reg-Set “Write_Data” (write on negative edge).