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## ECE 3055, COMPUTER NETWORKS, QUIZ 1

Quiz No. 1: Feb. 14, 2000
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## RULES.

i This quiz is closed book, except for one personally prepared handwritten sheet.
ii. Calculators may be used.
iii Answer all questions and show all work to receive full credit.
iv All questions have the same weight. ( 20 Points). All sub-questions within a question are weighted equally.
$v \quad$ Please do not ask the proctors any questions during the exam about exam questions. Part of the test is understanding the question as written, without supplemental information. If you feel additional data is needed to solve the problem, make (and state) an assumption and then work the problem.

## Question 1 - Workstation Evolution.

From 1985 to 2000 the processing speed of desktop workstations (PCs) increased by a factor of 1000. The clock speed increased from 5 to 300 MHz . The data bus width increased from eight bits to 32 bits. For the answers below, assume simple linear relationships and round answers to an integer.
[ 60 ] By what factor did the PC processing power increase due to clock speed?
$300 / 5=60$
[ 4 ] By what factor did the PC processing power increase due to a bus width?
$32 / 8=4$
[ 4 ] By what factor did the PC processing power increase due to other developments?
$1000 /(60 * 4)=4$
[ pipelining ] Name one of those other developments (inside the CPU chip).
[ cache memory ] Name one of those other developments (outside the CPU chip).
[ virtual memory ] Name a third development that allows a modern PC to run programs (or a number of programs) whose memory requirements are larger than the physical memory (RAM) in the machine.
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## Question 2 - Efficiency

The following is for a non-pipelined MIPS machine with a 50 ns clock cycle. ,
[ 50,000 ns ] How long would it take to execute 1000 instructions (answer in ns)?
[ 0 ] In 1000 instructions, 200 are branches of which 100 can have an instruction that does not depend on the branch placed after it. If $50 \%$ of the remainder are predicted correctly, how much time is wasted due to stalls or flushes.
\{ non-pipelined - no stalls \}
The following is for a fully pipelined MIPS machine with a 10 ns clock cycle.
[ 10,040 ns ] How long would it take to execute 1000 instructions if there are no data or structural hazards? \{ 1 instruction starts each clock cycle \}
[ 10,040 ns ] Suppose load-word instructions take 5 cycles, but all other instructions complete in 3 cycles. How long would it take to execute 1000 instructions if there are no data or structural hazards? \{ 1 instruction starts each clock cycle \}
[ 400 ns ] In 1000 instructions, 200 are branches of which 120 can have an instruction that does not depend on the branch placed after it. If $50 \%$ of the remainder are predicted correctly, how much time is wasted (added) due to stalls or flushes.

## Question 3 - Definitions

Match up the following possible situations with the names below.
A. Immediate use of a register value that was just written.
B. Feeding back the output from the ALU to one of the ALU inputs.
C. An ALU overflow.
D. A branch instruction whose direction was not predicted.
E. Predicting a branch direction based on previous directions.
F. Halting the IF and EX stages while letting other stages execute.

| $[$ | D | ] | Control hazard |
| :--- | :--- | :--- | :--- |
| [ A | ] | Structural hazard (Data dependency ) |  |
| [ | F | ] | Stall or bubble |
| $[$ | E | ] | Dynamic branch prediction |
| [ | B | ] | Forwarding |

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## Question 4 - Parts of the CPU

Using the attached diagram of the Pipelined MIPS processor which has major components labeled with letters, write the letter next to the component names below. Use an " X " if the component is not shown on the diagram.

| E | ] | Control |
| :---: | :---: | :---: |
| [ N | 1 | ALU |
| [ J | ] | Forwarding unit |
| [ H | ] | Comparitor ( $<,=,>$ ) for early branch detection |
| [ 1 | ] | Pipeline Register |
| [ B | ] | Instruction Memory |
| [ A | ] | Program Counter (Instruction Pointer Register) |
| [ X | ] | Virtual to Page Address Translation cache |
| [ X | ] | Dynamic branch prediction table |
| [ K | ] | Data Memory |

## Question 5-Caching and Virtual Memory

For an n -word wide memory cache, the 32-bit memory address* is divided into four parts:
( Part A | Part B | Part C | Part D )
[ C ] Which part indicates the word offset in the wide cache memory?
[ B ] Which part (letter) is used for the index (address) of the cache memory?
[ A ] Which part is compared to the tag value stored in the cache memory?
[ D ] Which part is not used for addressing words in memory?
[ A ] Which part is translated from the vitual page address (more than any other)?
*using the standard convention, as in the book, that the highest-order bit is on the left.

