ECE 3055 Laboratory Assignment 4
Due Date: Thursday, March 30

In this lab, you will use Java or C/C++ to write a program that will compare the performances of the MIPS multi-cycle and pipelined datapaths for varying cache characteristics. Calculate and plot the speed-up of the pipelined datapath relative to the multi-cycle datapath for a data cache miss rate ranging from 0.00 (0%) to 0.20 (20%) in steps of 0.01. Assume instruction cache miss rate is fixed at 0.02 (2%). Plot the speed-up for cache miss penalties of 5, 10, 20, and 50 cycles for both read and write misses.

You do not have to write code to plot the data, only to calculate it. The plotting can be done by any method you wish, e.g. by hand or with an available plotting program.

Assume the following:

1) Clock cycles are the same for both datapaths
2) Instruction frequencies are:
   - branches: 10%
   - loads: 20%
   - stores: 10%
   - other: 60%
3) Cycles per instruction for the multi-cycle datapath are:
   - branches: 3 cycles
   - loads: 5 cycles
   - rest: 4 cycles
4) For the pipelined datapath:
   - the branch penalty is 1 cycle and there is no branch prediction
   - load word hazards cause a 1-cycle stall and 2/3 of the loads cause hazards
   - all other data hazards are handled without stalling by the forwarding hardware
   - no compiler optimizations are done
5) You can ignore the 4-cycle start-up time of the pipeline in your calculation.

In your demonstration to the TA, your program should prompt the user to input the data cache miss rate and the miss penalty and then it should output the speed-up. You should turn in a cover sheet with your name, section, date, and assignment number; the plots that you generated according to the above instructions; your code; and a 1-paragraph write-up analyzing the plots. Be prepared to explain the behavior shown in your plots to the TA and also to explain how you calculated speed-up.

You may want to study the "Calculating Cache Performance" example on page 565 of Patterson and Hennessy before beginning the assignment, **page 397 for the non-pipelined multi-cycle datapath.**