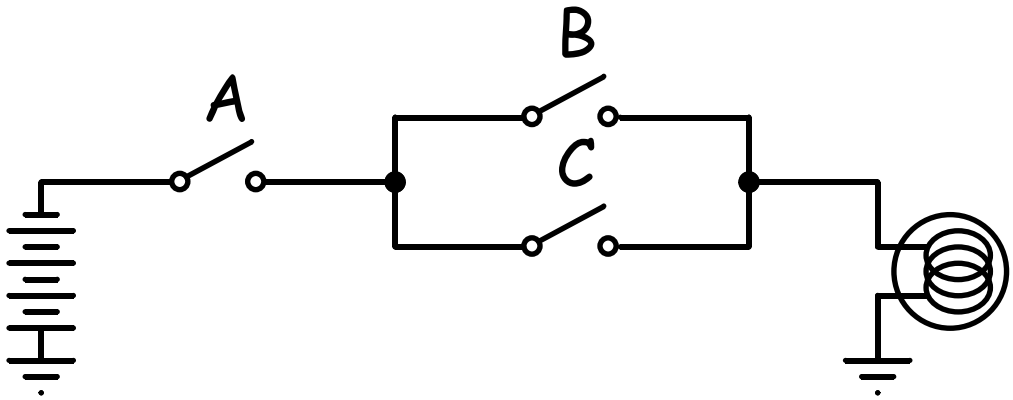
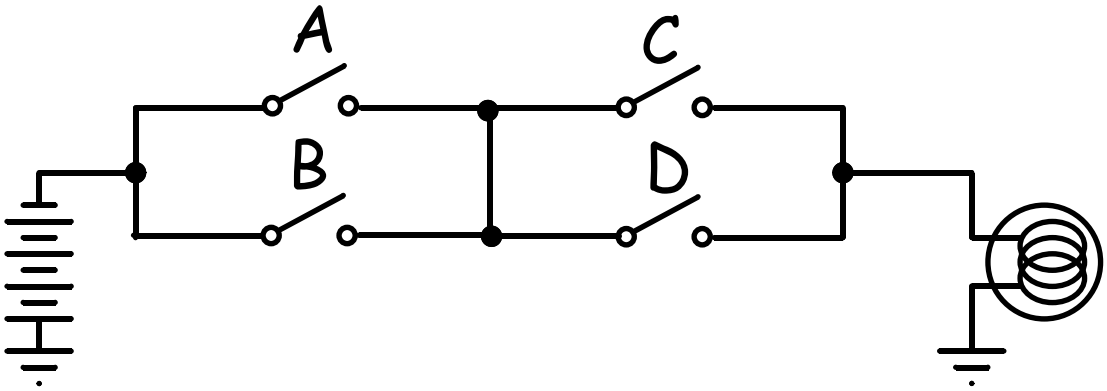
# Switch Design Problems

**Switches-1:** For each circuit below, write the logical function describing when the light is on.

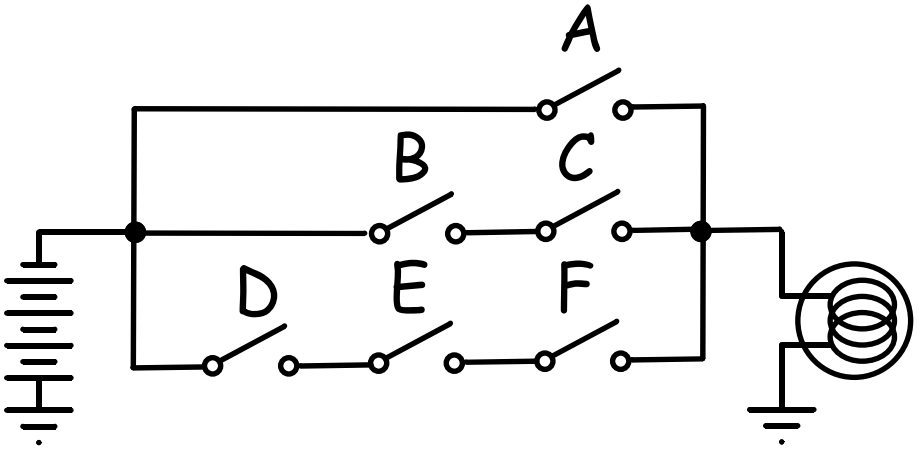
a)




b)




c)



**Switches-2:** Design a switch level implementation of the following equations using NFETs and PFETs only. Assume that the complement of each signal is available.

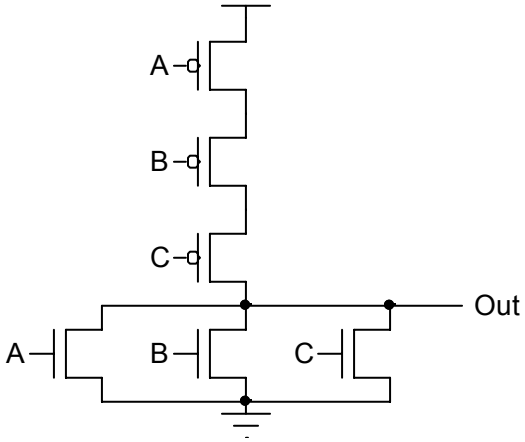
a) $f = \overline{A}$
b) $f = A \cdot B$
c) $f = A + B$
d) $f = \overline{A \cdot B}$
e) $f = \overline{A + B}$
f) $f = \overline{A} \cdot B + A \cdot \overline{B}$

**Switches-3:** Design a switch level implementation of the following equations using NFETs and PFETs. Assume that the complement of each signal is available.

a) $f = B \cdot (A + C)$
b) $f = \overline{A} \cdot B + C$
c) $f = A \cdot B + C \cdot D$
d) $f = \overline{A} \cdot (\overline{B} + C \cdot D)$
e) $f = \overline{A} \cdot (\overline{B} + \overline{C})$
f) $f = (A + B) \cdot (B + C)$
g) $f = A \cdot \overline{B} \cdot (\overline{C} + D)$
h) $f = \overline{A} \cdot (\overline{B} \cdot C + \overline{D})$
i) $f = A \cdot B + \overline{A} \cdot \overline{B} + \overline{B} \cdot C$
j) $f = \overline{A} \cdot (B \cdot \overline{C} + \overline{D} \cdot E)$
k) $f = (A + B + C) \cdot (D + E)$
l) $f = \overline{\overline{A} \cdot B + C + \overline{D} \cdot E}$
m) $f = \overline{A + \overline{B} \cdot D + C}$
n) $f = (A + \overline{B} + E \cdot \overline{F}) \cdot (C \cdot D + G)$
o) $f = \left( \overline{A + \overline{B} + C} + D \right) \cdot (E + F)$

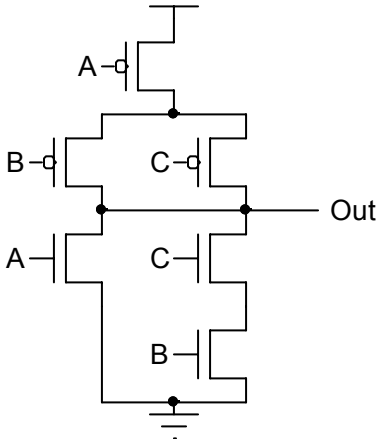
**Switches-4:** Determine the Boolean expression and complete the truth table for each circuit below.

a)



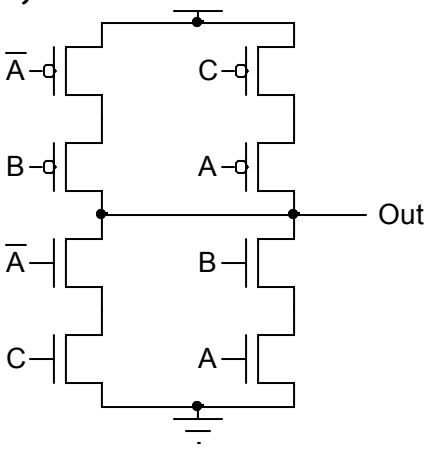

| A | B | C | Out |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

b)



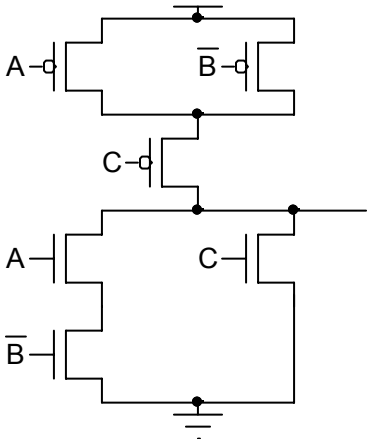

| A | B | C | Out |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

c)



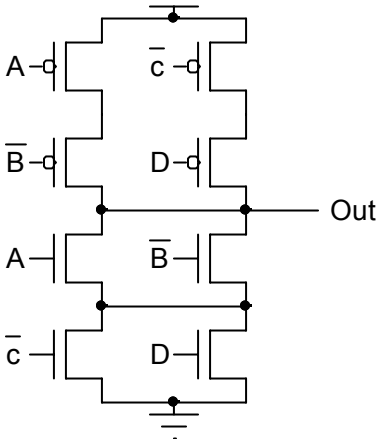

| A | B | C | Out |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

d)



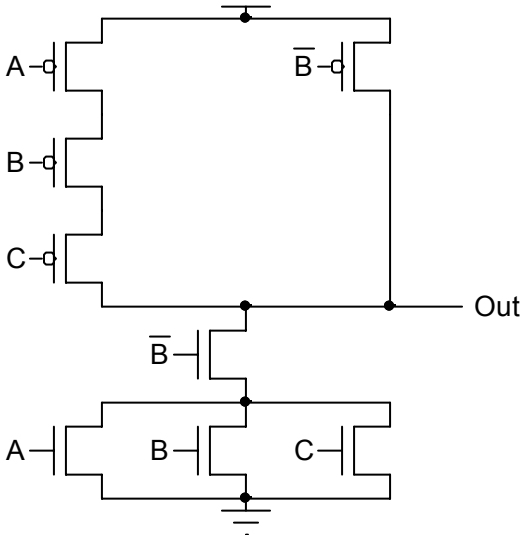

| A | B | C | Out |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

e)



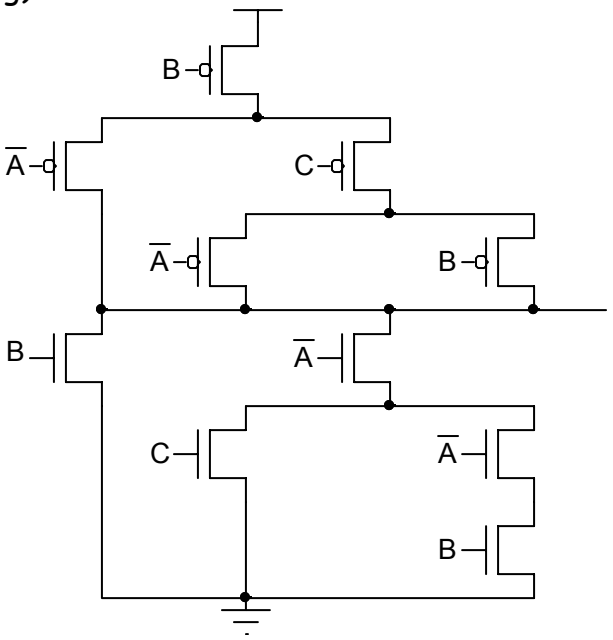

| A | B | C | D | Out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | |
| 0 | 0 | 0 | 1 | |
| 0 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | |
| 0 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 0 | |
| 0 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 0 | |
| 1 | 0 | 0 | 1 | |
| 1 | 0 | 1 | 0 | |
| 1 | 0 | 1 | 1 | |
| 1 | 1 | 0 | 0 | |
| 1 | 1 | 0 | 1 | |
| 1 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 1 | |

f)



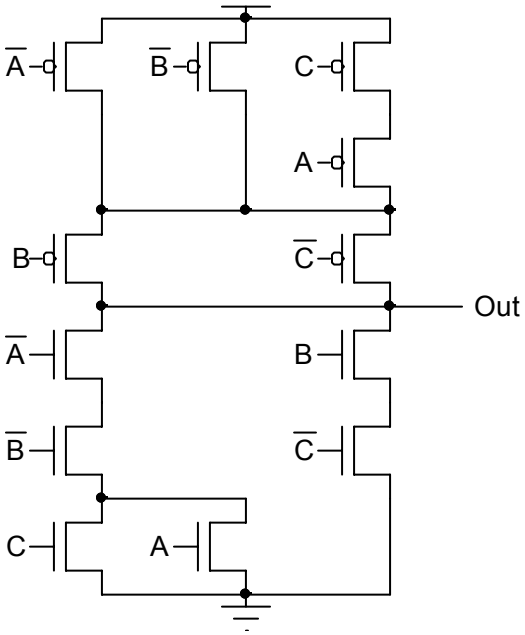

| A | B | C | Out |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

g)



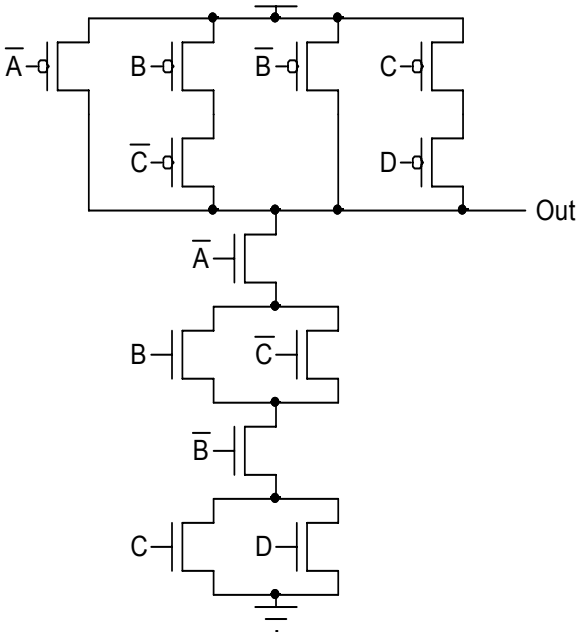

| A | B | C | Out |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

h)



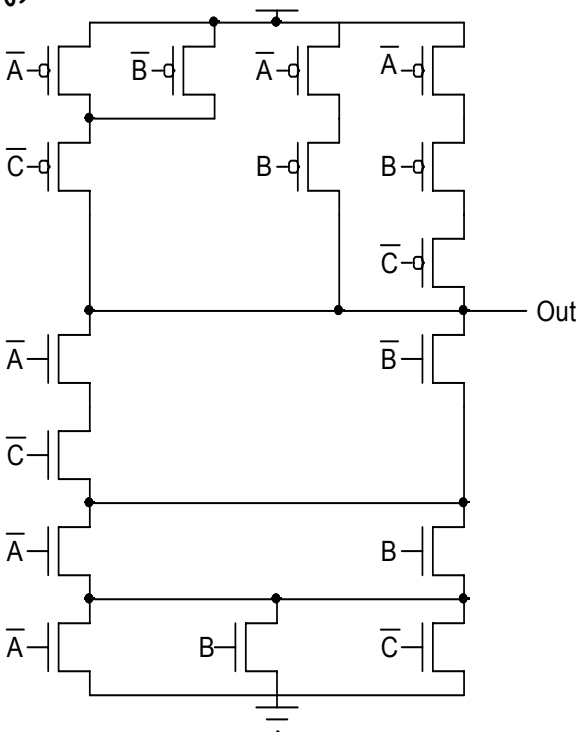

| A | B | C | Out |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

i)



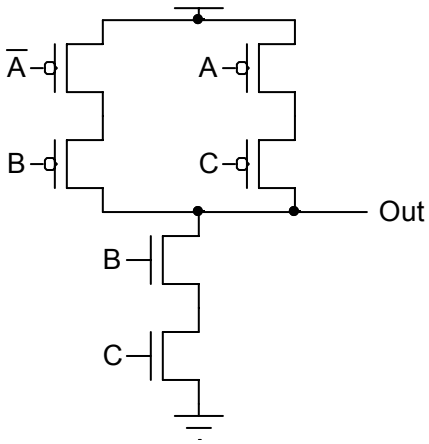

| A | B | C | D | Out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | |
| 0 | 0 | 0 | 1 | |
| 0 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | |
| 0 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 0 | |
| 0 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 0 | |
| 1 | 0 | 0 | 1 | |
| 1 | 0 | 1 | 0 | |
| 1 | 0 | 1 | 1 | |
| 1 | 1 | 0 | 0 | |
| 1 | 1 | 0 | 1 | |
| 1 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 1 | |

j)



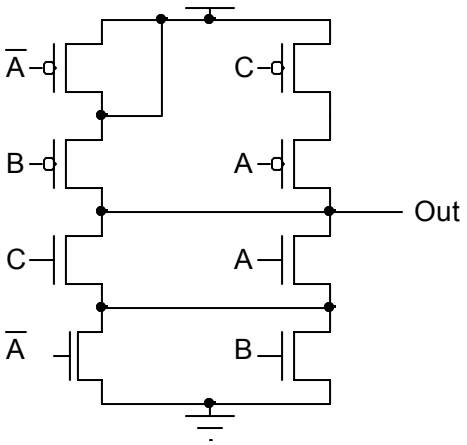

| A | B | C | Out |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

k)



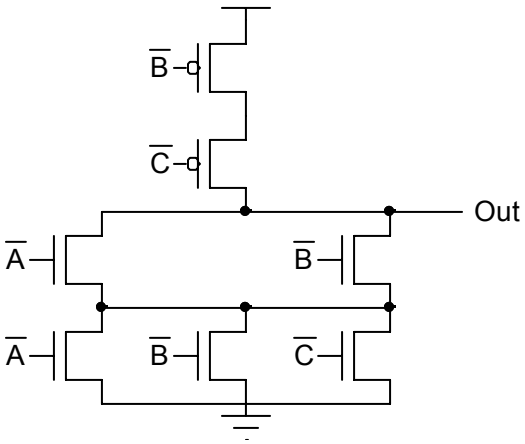

| A | B | C | Out |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

l)




| A | B | C | Out |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

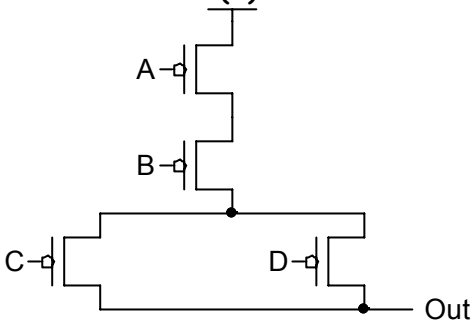
m)



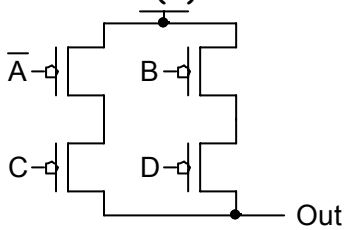

| A | B | C | Out |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

**Switches-5**: Complete the following partial circuits, and then determine the equations representing the complete circuits.

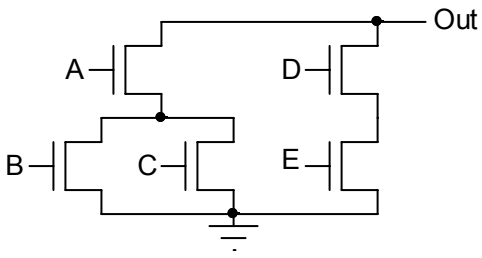
(a)



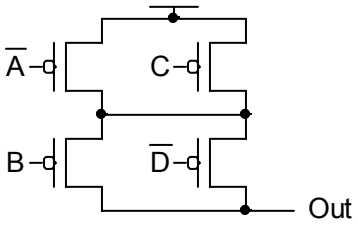

(b)



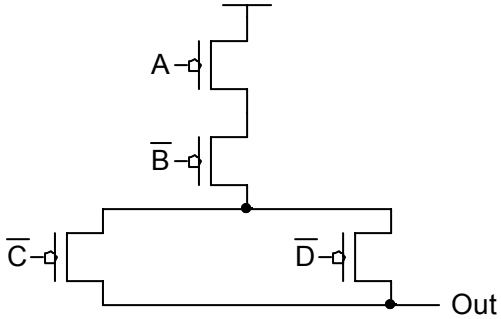

(c)



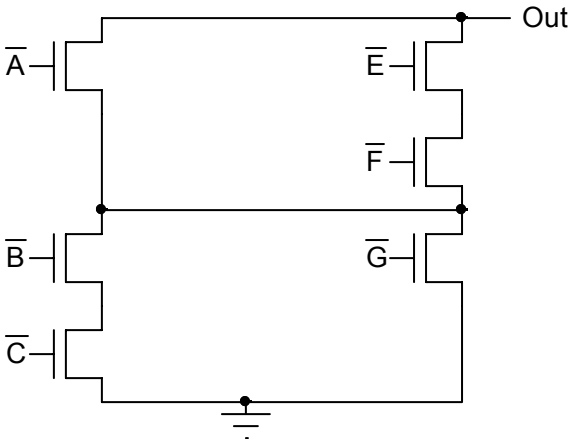

(d)



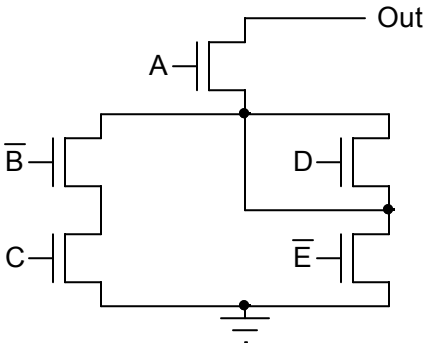
(e)



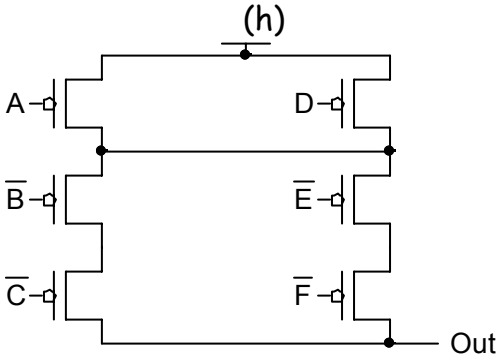

(f)



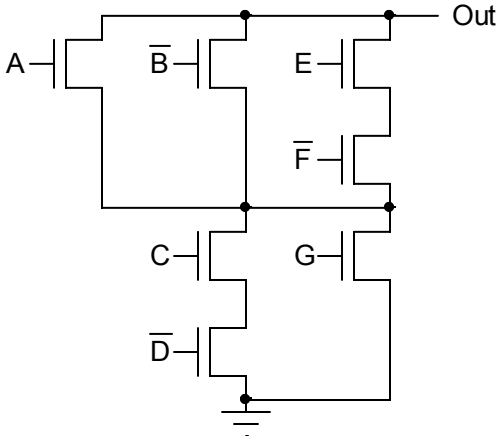

(g)



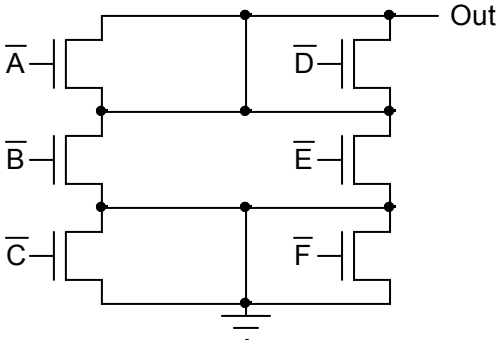

(h)



(i)




(j)




(k)