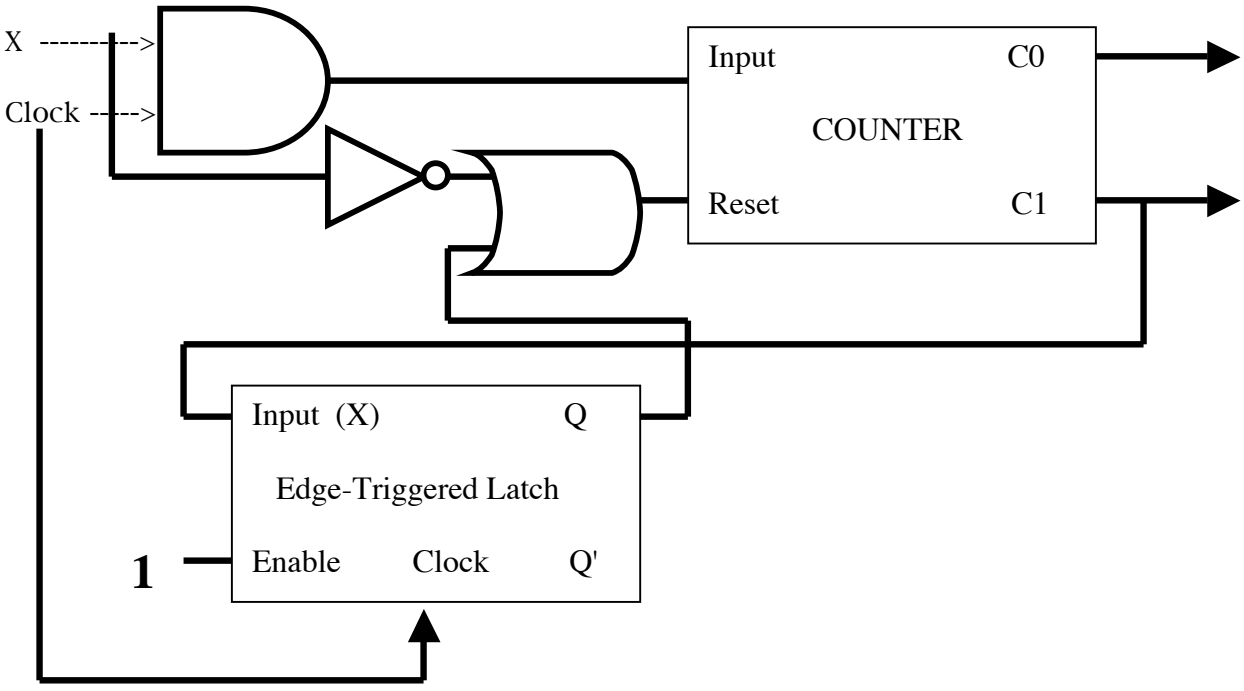
Bring this homework to class on Friday March 26.

HW-7. Finite State Machine - Circuit Design

1. Design a synchronous circuit with a two-bit counter (output is C1,C0, negative-edge triggered) that counts the number of 1's in a row (from input X). When X=0, or a third "1" in a row is detected, resets the counter output, C1, C0, to 0,0.

Example Input (X) and output (Ci):

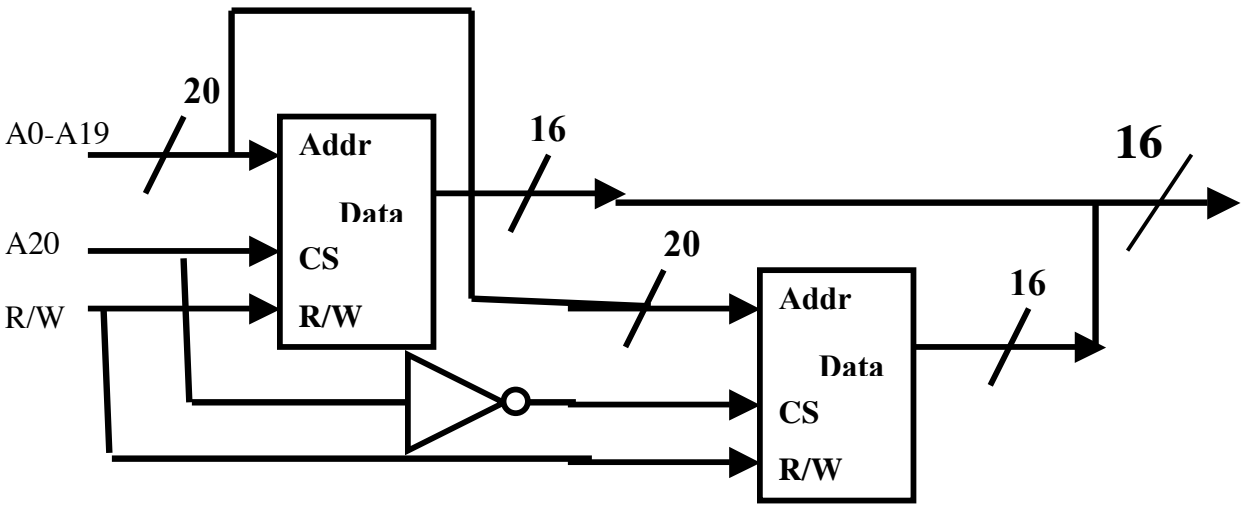
```
X:      0   1    1   1   1   0   0   1   0   1   1   0   1   1   1   0
C1,C0   0   01   10  00  01  00  00  01  00  01  10  00  01  10  00  00
```



2. Complete the table below. A "2M x 16" memory has 2M words of 16 bits.

Memory	Total Bits	# of addresses	# of address lines	# of data lines
4M x 8	**32M**	**4M**	**22**	**8**
1M x 32	**32M**	**1M**	**20**	**32**
128K x 16	**2M**	**128K**	**17**	**16**
1K x 4	**4K**	**1K**	**10**	**4**

B. 3. Show how to connect these 1M x 16 chips to make a 2M by 16 memory.



The inverter is used as a 1:2 multiplexer (one of 2 outputs is "1" based on a one-bit binary code.