# ECE-2030b – Homework 4

## Due Monday Oct. 7 before class

The answers to these problems will be posted after the due date.

While homework problems are not graded on a right or wrong basis, credit will not be given for homework problems that are left blank or which do not demonstrate a reasonable attempt was made to work them.

Problems where the answer appears to have been copied (and where intermediate work would normally be shown) are also in jeopardy of receiving a lower grade.

Notes: PDF files with 2 sides per page are available. Links to them are in the right-hand column of the class schedule, www.csc.gatech.edu/~copeland/2030/schedule.html

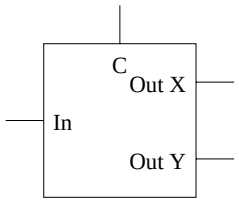
**Demultiplexers**

**Part A** Implement a 1-to-2 demultiplexer (described in the truth table below) using basic gates. Be sure to label the inputs, $IN$, $C$, $Out_A$, and $Out_B$.

| $IN$ | $C$ | $Out_A$ | $Out_B$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |

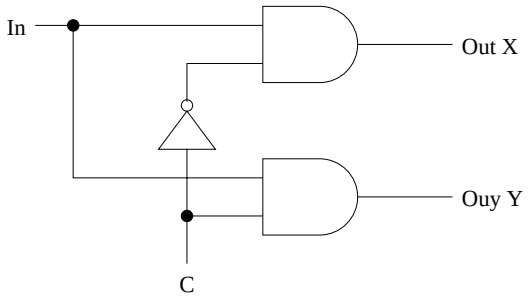
**Part B** Now design a 1-to-4 demultiplexer, define in the truth table below, using 1-to-2 demultiplexers. Be sure to label the inputs, $IN$, $C_0$, $C_1$, $Out_A$, $Out_B$, $Out_C$, and $Out_D$. Use this icon for your one to two demultiplexer.

| $IN$ | $C_1$ | $C_0$ | $Out_A$ | $Out_B$ | $Out_C$ | $Out_D$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

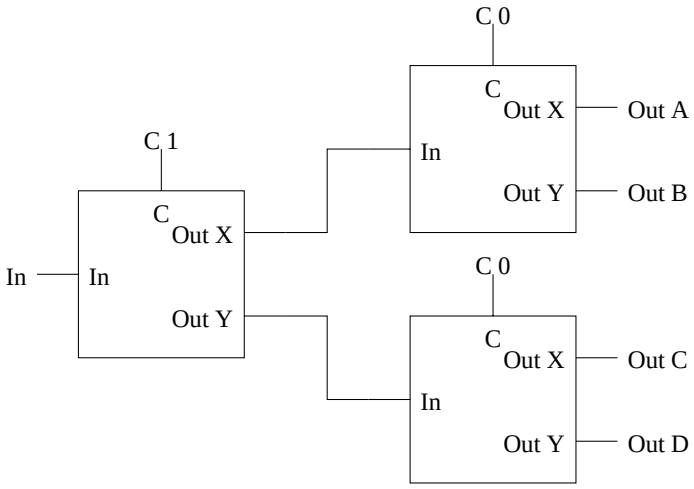


**Demultiplexers**

**Part A**




**Part B**



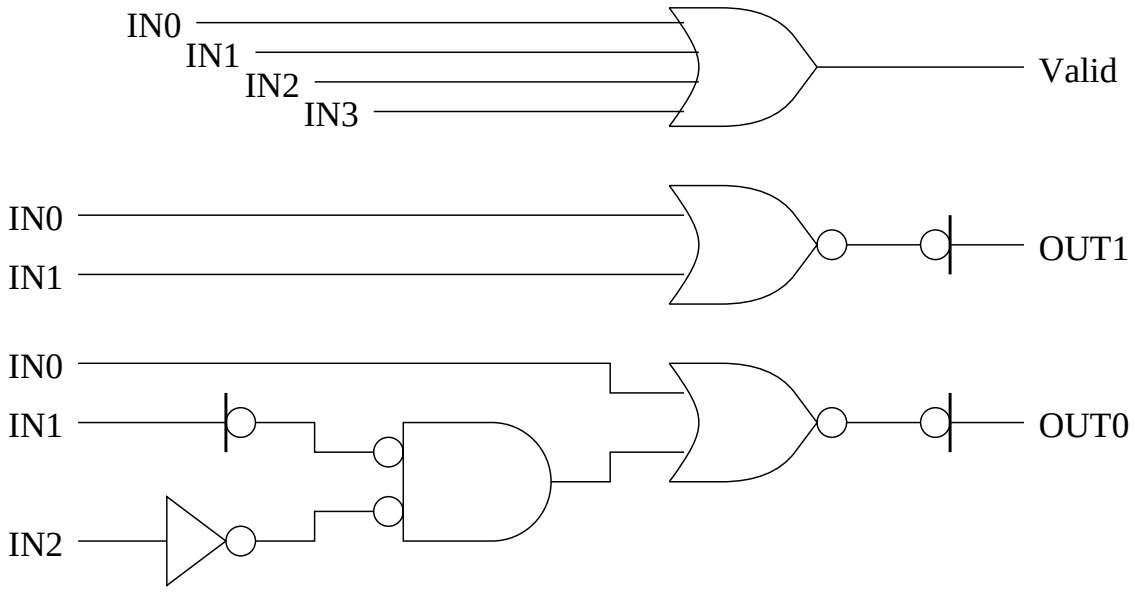
**Priority Encoders**

**Part A** Complete the following truth table for a priority encoder. Assume the priority order (from highest to lowest) is $IN_2$, $IN_0$, $IN_3$, $IN_1$.

| $IN_3$ | $IN_2$ | $IN_1$ | $IN_0$ | $OUT_1$ | $OUT_0$ | $Valid$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | X | X | 0 |
| X | 0 | X | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| X | 1 | X | X | 1 | 0 | 1 |
| 1 | 0 | X | 0 | 1 | 1 | 1 |

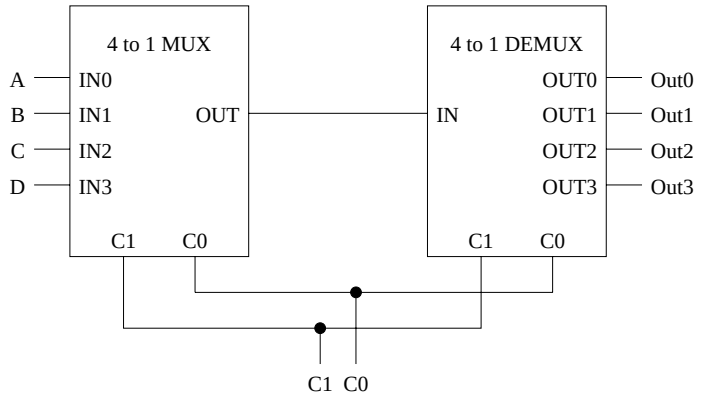
**Part B** Implement the following priority encoder using basic gates (AND, OR, NAND, NOR, and NOT). Label all inputs and outputs.

| $IN_3$ | $IN_2$ | $IN_1$ | $IN_0$ | $OUT_1$ | $OUT_0$ | $Valid$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | X | X | 0 |
| X | X | X | 1 | 0 | 0 | 1 |
| X | X | 1 | 0 | 0 | 1 | 1 |
| X | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 |



**Multiplexer Demultiplexer**

Complete the truth table for the circuit below. Assume the four inputs to the multiplexer are A, B, C, and D.



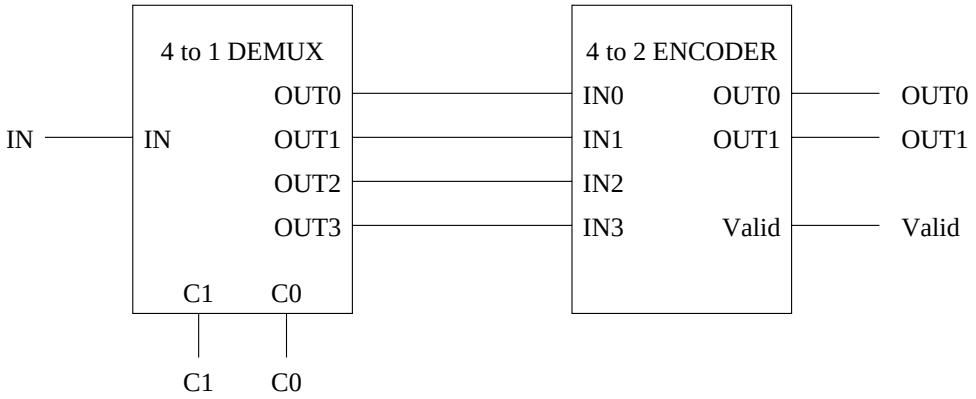

| $In_3$ | $In_2$ | $In_1$ | $In_0$ | $C_1$ | $C_0$ | $Out_3$ | $Out_2$ | $Out_1$ | $Out_0$ |
|---|---|---|---|---|---|---|---|---|---|
| D | C | B | A | 0 | 0 | | | | |
| D | C | B | A | 0 | 1 | | | | |
| D | C | B | A | 1 | 0 | | | | |
| D | C | B | A | 1 | 1 | | | | |

**Multiplexer Demultiplexer**

| $In_3$ | $In_2$ | $In_1$ | $In_0$ | $C_1$ | $C_0$ | $Out_3$ | $Out_2$ | $Out_1$ | $Out_0$ |
|---|---|---|---|---|---|---|---|---|---|
| D | C | B | A | 0 | 0 | 0 | 0 | 0 | A |
| D | C | B | A | 0 | 1 | 0 | 0 | B | 0 |
| D | C | B | A | 1 | 0 | 0 | C | 0 | 0 |
| D | C | B | A | 1 | 1 | D | 0 | 0 | 0 |

**Demultiplexer Decoder**

Complete the truth table for the circuit below. Assume unselected outputs from the demultiplexer are zero.




| $IN$ | $C_1$ | $C_0$ | $Out_1$ | $Out_0$ | Valid |
|---|---|---|---|---|---|
| 0 | X | X | | | |
| 1 | 0 | 0 | | | |
| 1 | 0 | 1 | | | |
| 1 | 1 | 0 | | | |
| 1 | 1 | 1 | | | |

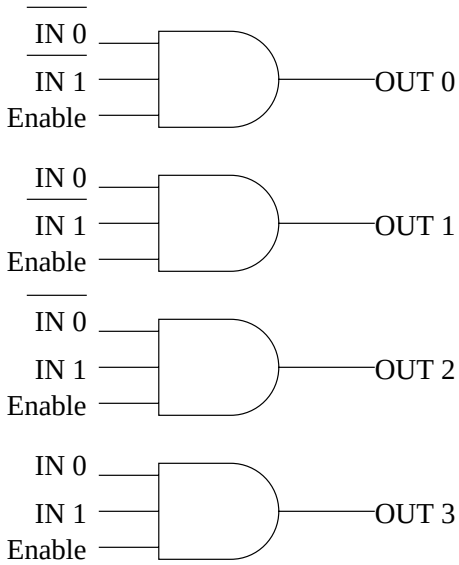
**Demultiplexer Decoder**

| $IN$ | $C_1$ | $C_0$ | $Out_1$ | $Out_0$ | Valid |
|---|---|---|---|---|---|
| 0 | X | X | X | X | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

**Decoders**

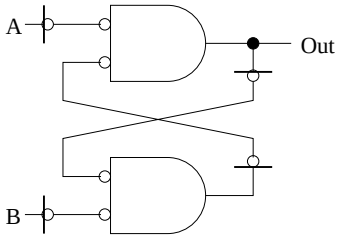
Implement a two to four decoder with enable using only basic gates (AND, OR, NAND, NOR, and NOT). Assume that you have the input signals and their complements. Be sure to label the inputs $IN_0$, $IN_1$, and *Enable*, and the outputs $OUT_3$, $OUT_2$, $OUT_1$, and $OUT_0$.

**Decoders**


IN 0
IN 1
Enable
OUT 0
IN 0
IN 1
Enable
OUT 1
IN 0
IN 1
Enable
OUT 2
IN 0
IN 1
Enable
OUT 3

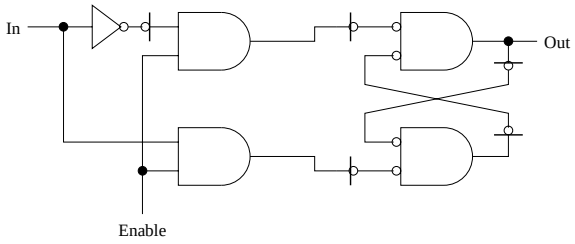
**Transparent Latches**

**Part A** Complete the truth table to describe the circuit below:



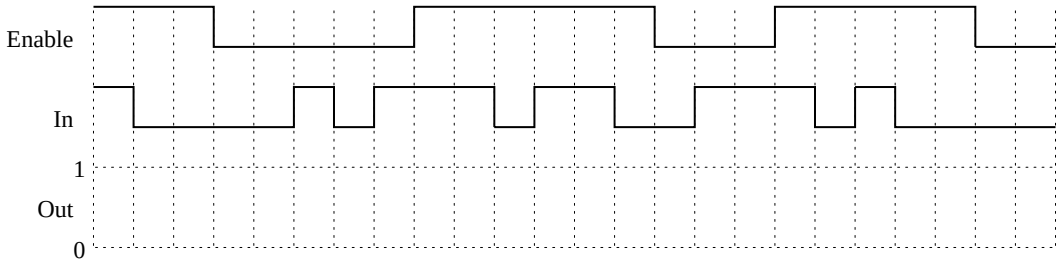

| A B | Out |
|---|---|
| 0 0 | |
| 1 0 | |
| 0 1 | |
| 1 1 | |

**Part B** Now consider a transparent latch based on this circuit (show below). How many transistors are used in this implementation?




_____transistors

**Part C** Complete the timing diagram for the latch output based on the specified inputs.

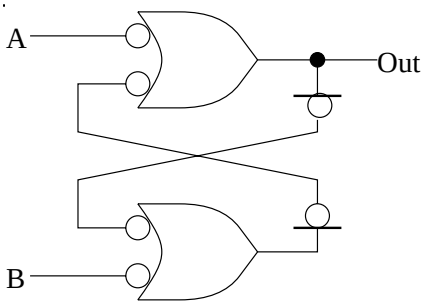



**Part D** Design a latch using four 2-input NOR gates and two inverters. Be sure to label the signals In, Out, and Enable.

**Part E** Design a transparent latch using four 2-input AND gates and five inverters. Be sure to label the signals In, Out, and Enable.

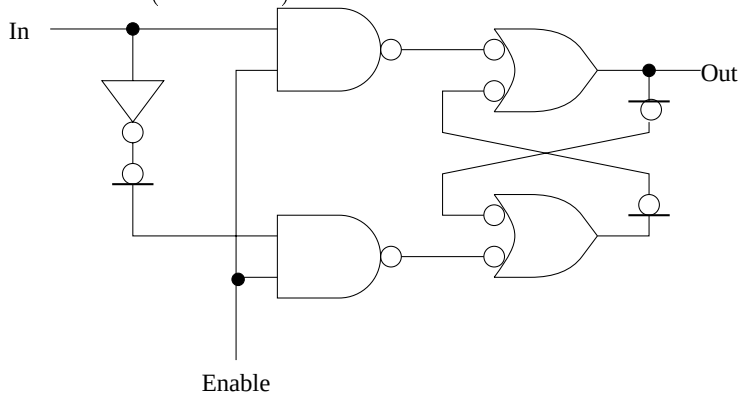
**Part F** Design a transparent latch using only four 2-input OR gates and six inverters. Be sure to label the signals In, Out, and Enable.

**Part G** Complete the truth table to describe the circuit below. Also indicate which states denote RESET, SET, and HOLD.



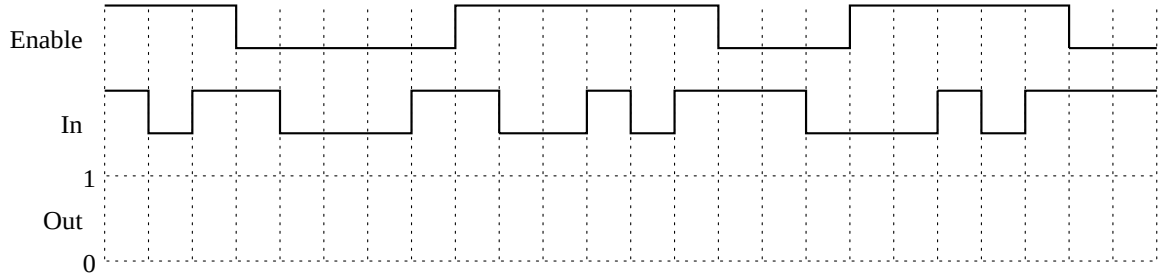

| A B | Out |
|---|---|
| 0 0 | |
| 1 0 | |
| 0 1 | |
| 1 1 | |

**Part H** Now consider a transparent latch based on this circuit (shown below). How many transistors are used in this implementation (show work)?




_____transistors

**Part I** Complete the timing diagram for the latch output based on the specified inputs.

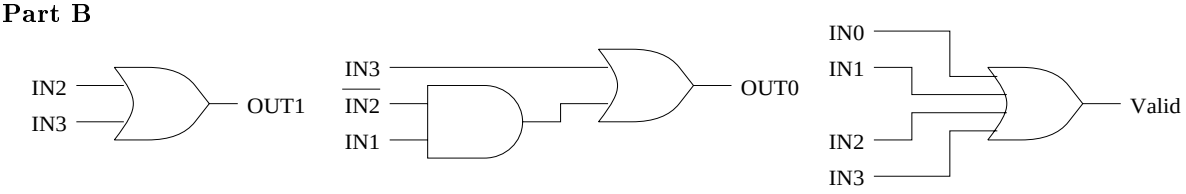


**Encoders**

**Part A**

| $IN_3$ | $IN_2$ | $IN_1$ | $IN_0$ | $OUT_1$ | $OUT_0$ | $Valid$ |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| X | 1 | 0 | 0 | 1 | 0 | 1 |
| X | X | 1 | 0 | 0 | 1 | 1 |
| X | X | X | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | X | X | 0 |

**Part B**




**Part C**

$IN_2$ highest, $IN_0$ 2nd highest, $IN_3$ 3rd highest, $IN_1$ lowest

**Part D**