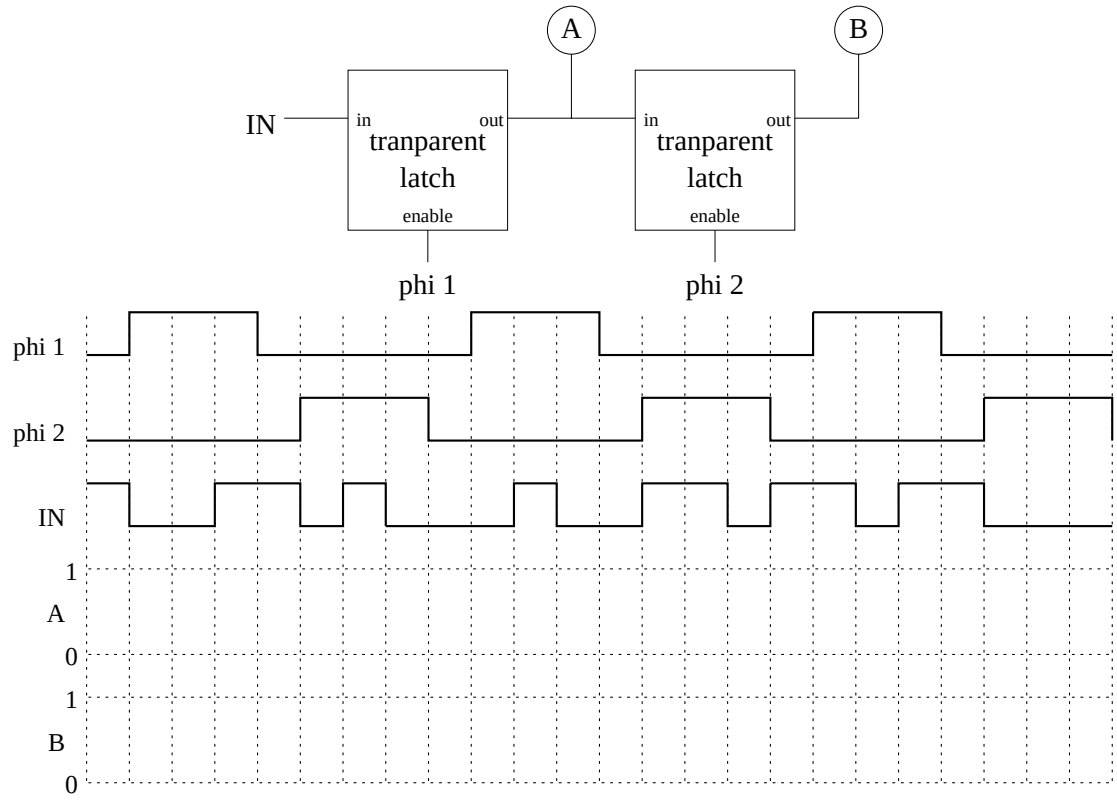
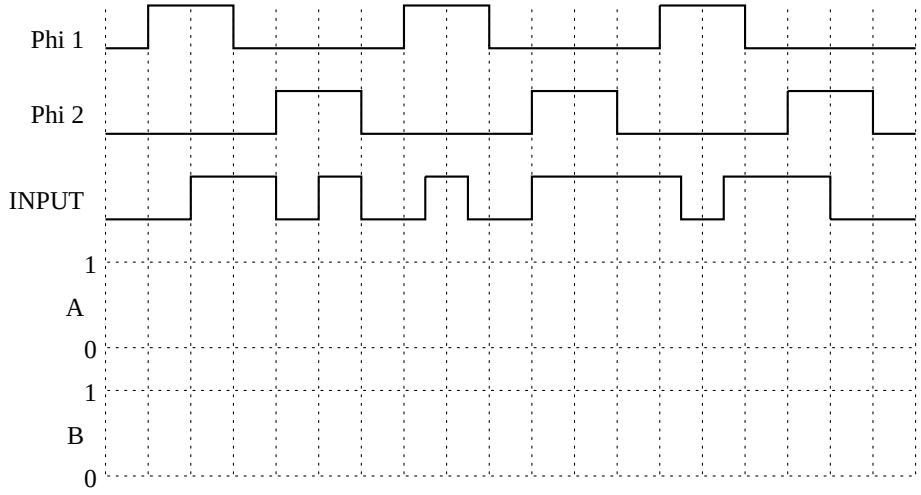
Registers

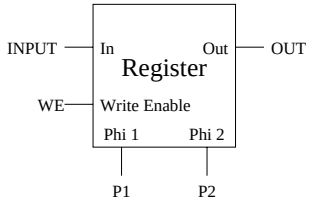
Part A Complete the timing diagram for the REGISTER shown below by determining test points A and B. Assume both latch states are initially zero.



Part B Complete the following timing diagram for the circuit above. Assume all latch values are initially zero.

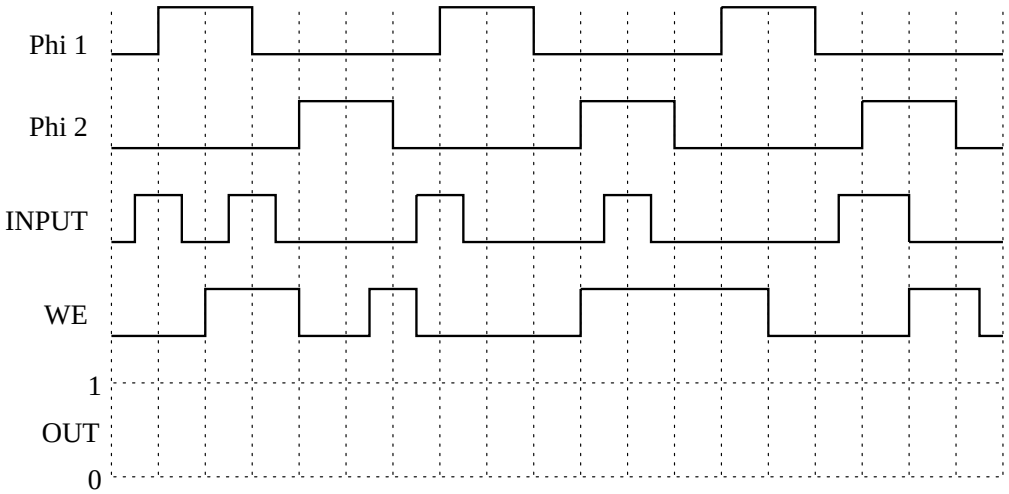


Part C Implement a **register with write enable** (shown below in icon form), using only transparent latches, NAND, NOR, AND, OR, and NOT gates. Use mixed logic design methodology. You do **not** have to implement transparent latches from basic gates.



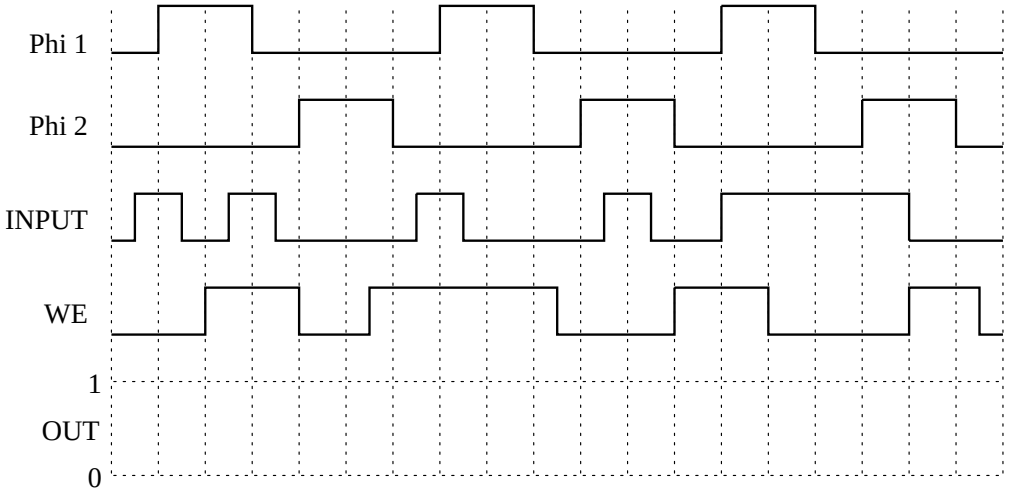
Part D On the timing diagram below, draw a vertical line at each time where a new input value is sampled by the register. The new value should be different from the current value.

Part E Now complete the timing diagram for this register based on the specified inputs. Assume all internal storage is initially zero. Ignore gate propagation delay.



Part F On the timing diagram below, draw a vertical line at each time where a new input value is sampled by the register. The new value should be different from the current value.

Part G Now complete the timing diagram for this register based on the specified inputs. Assume all internal storage is initially zero. Ignore gate propagation delay.



Memory Systems

Part A Many PCs today have 16 million address memory systems with 8 bit words (bytes). Suppose they are built using one million address by four bit word DRAM memory chips. Answer the following questions about the memory systems design.

How many address lines does the memory system require? _____

How many data lines does the memory system require? _____

How many address lines does the DRAM memory chip require? _____

How many memory chips are required for the system? _____

What kind of address decoder is required? _____ to _____

Part B A new memory part is now available, a **four million** address by **four bit** word DRAM chip. Reconsider the design if this chip is used to build the same memory system.

How many address lines does the DRAM memory chip require? _____

How many memory chips are required for the system? _____

What kind of address decoder is required? _____ to _____

Part C The original IBM PC introduced in 1980 was socketed for **16 thousand** address by **one bit** word DRAM memory chips. Reconsider the design if this chip is used to build the same memory system.

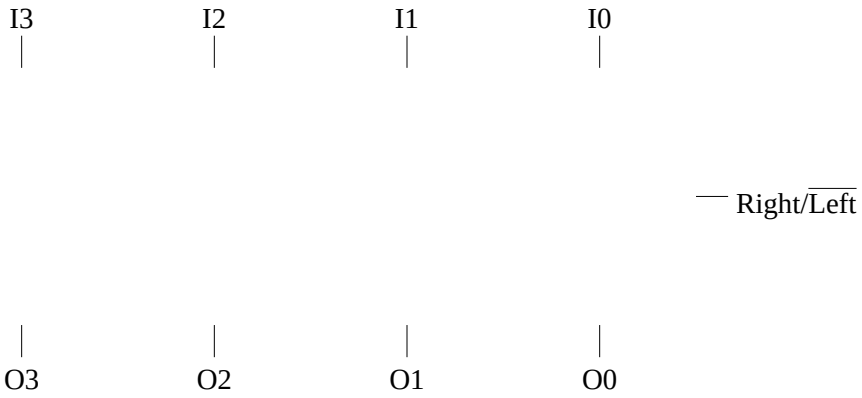
How many address lines does the DRAM memory chip require? _____

How many memory chips are required for the system? _____

What kind of address decoder is required? _____ to _____

Shift Unit

Part A Design a four bit arithmetic shifter that can shift one bit left or right using only pass gates and one inverter. You only need to connect to the active high side of each pass gate.



Part B Using the inputs and outputs of the shift unit in part A, design logic which produces an error signal when shifting four bit two's compliment numbers. The output of this logic *Error* is high when an error results from the shift. Note: rounding fractional number is not an error.